Recent Topic in Electrochemical Engineering  
– Micro Size Electrodeposition Technology

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ABSTRACT

Micro size electrodeposition technology is the most recent topic in the field of electrochemical engineering. In this report, introduction is given on both the most recent fields and future targets of this micro size electrodeposition technology. The year v.s. characteristics length of the electrodeposited feature is plotted on the semi-log graph. The 90 degree bent on this graph in 1980 was driven by the application of electrodeposition technology to the conductors and connectors of electronics devices. The electrodeposited copper conductors line width used in microprocessors have 1/1000 of the diameter of the human hairs (0.1 μm).

Recent micro size electrodeposition technology is reviewed. The build up printed circuit board, super connect (interconnection between chips and inter-poser) and the copper Damascene electrodeposition used for the conductors inside of the chips (back end line). Also the future targets of this technology are discussed for the FERAM capacitor and MEMS on-chip switch.

KEY WORDS

Electrodeposition, Electro Chemical Engineering, Copper Damascene, Packaging, Bumping

INTRODUCTION

In both the AIChE and Electrochemical Society in the U.S., Electrochemical Engineering has traditionally been a strong field. Unfortunately, not in Chemical Engineering Society, Japan nor Electrochemical Society, Japan. The field of Electrochemical Engineering has been developed with industrial electrolysis such as copper winning electrolysis. However, most researchers in the field are focusing on the copper Damascene process - micro size electrodeposition technology, since the announcement of the successful development of copper conductor metallization process of microprocessor (Power PC 800) from IBM in 1999.

In the micro size electrodeposition, the amount of the electrodeposited is proportional to the current density (Faraday’s law). Hence the control of the current density is the most critical issue. The current density is the sum of the ionic mass transportation in the electrolyte (diffusion and convection), the electrolytic potential and the electrochemical reaction on the electrode. The basic current density equations are shown as follows.

\[ N_i = -z_i \mu_i F c_i \nabla \phi - D_i \nabla c_i + C_i \nu_i \]  \hspace{1cm} (1)

\[ \Sigma z_i c_i = 0 \]  \hspace{1cm} (2)

\[ i = i_0 \left[ \exp \frac{\alpha_i F}{RT} \eta - \exp \frac{\alpha_i F}{RT} \eta_0 \right] \]
Equation (1) represents the flux for the i-component ion(Ni) and Ni is the sum of the electrolytic potential and the ionic mass transportation of diffusion and convection. Equation (2) is the restricted condition of electrical neutrality of + and - ions. Equation (3) is the electrochemical reaction on the electrode and it is the sum of the anodic and cathodic reactions based on the Euling’s rate theory. These are basic equations used in the field of conventional chemical engineering, except that the electrolytic potential term in equation(1) and electrical neutrality condition of (2). The boundary condition of surface reaction is the Butler-Volmer equation(3).

Recently, these equations of (1), (2) and (3) become more and more miniaturized. They are applied to the field of nano-technology of the scale of 100 µm to 0.1 µm. Actual applications are the conductors and connectors of electronic devices such as the handy phones or note book personal computers. This chemical engineering field is named as the micro size electrodeposition technology.

1. HOW SMALL THE ELECTRODEPOosition TECHNOLOGY CAN GO

Figure 1 shows the history of miniaturization of electrodeposition technology. X-axis is the age and y-axis is the characteristics length of electrodeposited feature. Y-axis is log-scale and it is a semi-log plot. The Buda statue was build at the age of 757 in the city of Nara. Cu and Au were deposited on the Buda surface by means of Hg-amalgam method. The Buda has the height of about 30m, so that the first plot in Fig.1 is 30m in characteristic length and 757 in age.

The second technological evolution in electrodeposition technology is the Zn and Zn alloy galvanized(electrodeposited) steel sheets used for the corrosion protection of the automobile body. In order to pass the Canadian code(The regulation to restrict the corrosion amount of the automobile body in Canada), huge electro galvanizing lines were constructed in many steel mills in 1980. This galvanized steel sheet has the width of 1.6m, so that the second plot in Fig.1 is 1.6m in characteristic length and 1980 in age.

Finally, the electrodeposition technology goes into the electronics devices. The liquid crystal display(LCD) developed and comes into the market in the late 1980’s. The display components of LCD
are called as pixels. These pixels are driven by the driver IC and the driver IC sends the digital signals, which illuminate each individual pixel. To obtain the high resolution of LCD, narrower pitch and higher pin counts interconnection between LCD and the driver IC is an important technology. The electrodeposited gold bumps (metal bumps for the interconnection) has been used as the interconnection and they are still being used today. Bumps are the 100 µm size metal conductors and are commercially available from 1990.

Copper Damascene process started to be used for the conductors in microprocessor (Power PC 800) in 1999. This process had been developed at IBM research center from 1990. Copper has lower resistance compared to aluminum, so that copper is much better in higher frequency transmission. Copper conductors have been commonly used for the high-end microprocessor, such as Pentium-4. These copper conductors line widths are about 0.1 µm and their width is 1/1000 of the diameter of the human hairs (Diameter of hair is 100 µm).

Figure 1 is the plots of the year in AC and the characteristic length of the electrodeposits, such as Buda statue, steel sheet galvanizing, bumps and copper Damascene conductors. It is the semi-log plot, so natural phenomena should be in linear and one straight line. However, Fig.1 has 90 degree bent after 1980 and this bent shows the electrodeposition technology has been used for more and more smaller features after 1980. The driving force of this miniaturization is the recent applications of electrodeposition to the electronic devices.

2. RECENT TOPICS IN MICRO SIZE ELECTRODEPOSITION TECHNOLOGY

The micro size electrodeposition technology have conventionally been used in the interconnection between the chips and the printed circuit board and the printed circuit board itself. Let’s begin the recent topics from outside of the chips, such as build up printed circuit board, super connect (Interconnection between chips and inter-poser) and the copper Damascene electrodeposition used for the conductors inside of the chips (back end line).

The recent build up printed circuit boards are produced by both the panel plating (electrodeposition) and pattern plating. The panel plating has the disadvantage in forming finer conductors, since the conductors are formed by etching process (subtractive). Hence, the most recent research and developments are concentrated in the pattern plating process. The electrodeposited thickness of the conductors depends on the pattern density - dense or coarse. To obtain the uniformity in conductor thickness is typical research example in current distribution.

The super connect is the field of technology that fills the conductor width gap between the printed circuit boards (typically, 100 µm) and chips (less than 1.0 µm). Three dimensional packaging has been developed by ASET (Advanced Super Electronics Technology) and this three dimensional packaging is the typical example of the application of the super connect. This three
dimensional packaging is the technology to stack the chips in height direction (z-axis). In order to stack the chips, chip thinning technology (CMP) and through via formation technology are required. The through via are formed by copper electrodeposition deep via filling. The via have the size of 10 μ m X 70 μ m of aspect ratio of 7.0, which is very deep. My laboratory corroborates with ASET and succeeded in forming perfect filling within electrodeposition process time of 1.0hr. Figure 2 shows one of the cases of the perfect via filling.

The copper Damascene electrodeposition has been used for the conductors inside of the chips (back end line). This electrodeposition process is achieved by the combination of the inhibition and acceleration additive effects. Most researchers in electrochemical engineering in the US, recently, are focusing in this topic. The hottest research topic is the chemical mechanism and simulation of the acceleration effect with SPS (bis(3-sulfopropyl) disulfide) which is the accelerator. Dr. Moffat in NIST and other researchers are focusing on the SPS adsorption at the curvature formed at trench bottom during copper Damascene electrodeposition. They are proposing the curvature enhanced effect.

Our experimental data, however, deny this adsorption model and indicates the existence of the free accelerating complex which moves freely in the electrolyte. Figure 3 shows our experimental data. The narrower the opening width of the patterned electrode formed by photo resist, the higher the current density and more acceleration effect is observed.

Furthermore the copper electrodeposits formed within the 2 and 10 μ m do not exhibit the curvature and shows flat in shape. The curvature is not causing the acceleration effect. The free accelerating complex exists which was monitored electrochemically on the ring of the rotating ring disk electrode by Dr. Veerecken at IBM.

4. FUTURE TARGETS OF MICRO SIZE ELECTRODEPOSITION TECHNOLOGY

The micro size electrodeposition technology is going to be applied more and more to the conductors and connectors formation of electronics device. The application of micro size electrodeposition technology into the chip, not outside of the chip is the next generation application.

The Pt, Ir and Ru electrodes will be used in the next generation high inductance PZT capacitors (FERAM). Figure 4 is the example of Pt electrode and 0.05 μ m diameter Pt column is formed. Since the capacitance (C) is proportional to the area, column surface is necessary in order to enlarge the capacitor.
surface area. The electrodeposition is especially being interested, since it has much high speed film formation speed if compared to the dry processes such as sputtering.

The passive components of handy phones will be on-chipped and this development has been proposed by IBM. On-chip switch using MEMS technology is the typical example. This switch consists of the beam, actuation electrode and RF contact(Fig.5). The beam is actuated by the actuation electrode. The beam top starts to oscillate at the high RF frequency and contacts the actuation electrode with RF. This is how the RF frequency switch works. Numerous holes formed on the beam is to eliminate the sacrifice film underneath the beam. This beam should be good electrical conductor and, at the same time, the process temperature should be less than 400°C, since the beams are formed on-chip after fabrication of the IC processes. Hence these beams should be formed by the micro size electrodeposition technology.

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