Automatic optical heterodyne phase lock by microcomputer-assisted loop filter

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Abstract: This paper demonstrates signal light carrier automatic pull-in and phase-lock to an optical frequency comb reference by our newly developed microcomputer-assisted phase-lock loop circuit. The microcomputer utilizes a binary-search algorithm to alter the oscillation frequency of the slave laser and achieve rapid pull-in to the master laser. It achieves automatic phase-locking time of 0.45 msec when the laser-diode frequency lies within the pull-in range of ±100 MHz. The single side band phase noise is just 1.8° at offset frequencies from 10 Hz to 5 MHz. This phase noise value is not expected to cause any power penalty with QPSK modulation.

Keywords: PLL, heterodyne, OFCR

Classification: Fiber-Optic Transmission for Communications

References

1 Introduction

The development of high-speed digital signal processors (DSP) in the last decade has enabled us to dramatically increase the spectral efficiency (SE) and transmission capacity of coherent optical communication [1, 2, 3]. DSP-based schemes can calibrate local oscillator (LO) frequency offset and estimate the relative phase between carrier and LO lights. They can also precisely compensate the linear and nonlinear fiber characteristics as well as replicate the sharp cutoff characteristics of electrical filters that yield, approximately, the Nyquist minimum bandwidth [4]. However, the SE is limited to just a single channel and in wavelength-division multiplexing (WDM) transmission, the SE degrades because of the bandwidth unnecessarily reserved to counter frequency fluctuation in each optical signal [5], even though the sharp cutoff filter can realize such dense channel spacing that the optical carrier frequency spacing matches the bandwidth of the sharp cutoff filter. Furthermore, the amount of digital signal processing is becoming a significant burden.

We have developed optical phase-lock loop (PLL) technology to realize the optical synchronous network and demonstrated stable homodyne detection for 20 Gbit/s QPSK signals [6]. If PLL technology is applied to not only long haul but also short distance optical transmission systems, we can enhance the light source frequency stability (which suppresses the unnecessary bandwidth usage), narrow its spectral line width, raise the symbol rate up to match the performance of pre-amplifiers and high-speed logic-ICs (which is not limited by analogue-to-digital conversion (ADC) speed), and reduce the DSP requirements. However, to the best of our knowledge, no paper has described the automatic pull-in and phase lock operation of slave LD frequency, which is necessary for optical communication systems.

This paper demonstrates light carrier automatic pull-in and phase-lock operation to an optical frequency grid comb reference (OFCR). The developed microcomputer-assisted (MA) analogue phase locked loop (PLL) circuit automatically pulls in and phase-locks an optical signal carrier to the OFCR. The MA-PLL starts to work by running a binary search algorithm (BSA) when the optical carrier frequency is set within $\pm 100$ MHz from some grid frequency, and locks the carrier phase to the OFCR within 0.45 milliseconds. The loop filter used in the MA-PLL is the same integral, lag and lead loop filter (I&LL-LF) as developed for 20 Gbit/s QPSK signal homodyne detection [6], with some changes to the circuit parameter values. Once signal carrier phase locking to the OFCR commences, it achieves the single-side band phase noise of 1.8° for offset frequencies from 10 to 5 MHz.

2 Microcomputer-assisted loop filter

In optical heterodyne phase locking to a reference light, the loop delay is the key to realizing a low phase noise PLL. The target of the phase noise, under 2°, is the value that causes no symbol error, as was demonstrated in reference 6 (Ref. 6). If an optical PLL circuit is to suppress the SSB phase noise to less than 2°, the loop bandwidth must exceed a few megahertz (MHz) even if the light source has spectral-linewidth of the order of kHz. When enlarging the loop bandwidth to over tens of MHz for wider spectral linewidth LD sources, the analogue circuit approach is superior to DSPs because DSPs that convert analogue to digital signals suffer excessive processing delays. Thus we adopted the analogue circuit approach and used a microcomputer to enhance operation performance.

A phase-frequency detector (PFD) and integral function of loop-filter are essential to the pull in and phase-lock operation. The PFD serves to pull the slave LD frequency into the reference and the integral circuit locks its phase stably to that of the reference. However, when the initial frequency difference between the slave and reference is large, pull-in operation may not complete due to saturation of the integral circuit. If the initial frequency difference can be set to within some allowable range, the slave LD frequency could approach the reference and its phase is locked by controlling its injection current.

![Image](413x328 to 526x421)

(a) MA-PLL circuit
(b) Photograph of MA-PLL prototype
(c) PFD’s characteristics and optical frequency behavior
(d) Binary search algorithm

Fig. 1. Microcomputer-assisted phase-lock loop and its binary search algorithm.
Fig. 1(a) shows the MA-PLL circuit with a photograph of our prototype in (b). The MA-PLL consists of a 32-bit, 96 MHz clock, microcomputer, I&LL-LF, PFD, photo-diode (PD) followed with trans-impedance amplifier (TIA), and an LD that emits the optical signal carrier. The OFCR in Fig. 1(a) provides the ITU-T standardized grid frequencies of $f(n) = 193.1\text{THz} + 25\text{GHz} \times n$; where, $n$ is integer from $-15$ to $15$ [7]. The red solid rectangle in Fig. 1(b) indicates the microcomputer, the yellow the I&LL loop filter, and the blue the PFD. The PD detects the beat frequency, $f_{\text{beat}}$, between the OFCR and the LD lights, and after comparing it with a 400 MHz RF reference, its phase error is extracted via the I&LL-LF. By feeding back the phase error information to the LD injection current, $I_{\text{bias}}$, the LD oscillation frequency of the light carrier can be phase-locked to the OFCR, where, $I_{\text{bias}}$ corresponds to $f_{\text{beat}}$.

The MA-PLL circuit starts to work when the slave LD frequency is set in a range of $\pm W_{\text{ini}}$; where, $W_{\text{ini}}$ is the maximum pull-in range specified for the MA-PLL. The PFD output is monitored and when $f(n) = f_{\text{ref}} < f_{\text{beat}}$, the PFD outputs negative voltage while it outputs positive when $f_{\text{beat}} < f(n)$, as shown in Fig. 1(c). Here, the BSA starts with the maximum variation of $W_{\text{ini}}$; where, $W_{\text{ini}}$ is integer range of $15$ to $15$ [7]. The red solid rectangle in Fig. 1(b) indicates the microcomputer set to $10\text{MHz}$. The AWG rejection ratio (CMRR) of over $43\text{dB}$ for a measurement bandwidth between DC and $1\text{MHz}$, as shown in Fig. 2(a). The optical frequency pull-in operation was monitored by utilizing our optical frequency discrimination circuit that had been developed for $20\text{Gb/s}$ QPSK homodyne detection, see Ref. 6, as shown in Fig. 2(b). The optical frequency discrimination circuit is comprised of a $12.5\text{GHz}$-spaced arrayed-waveguide grating (AWG), two pin-photodiodes followed by trans-impedance amplifiers and a differential amplifier. The set of electrical amplifiers forms a balanced amplifier that exhibits a common-mode rejection ratio (CMRR) of over $43\text{dB}$ for a measurement bandwidth between DC to $10\text{MHz}$. The AWG’s transmittance has a Gaussian profile of

$$f(x) = \exp\left\{-\frac{(x \pm x_0)^2}{2\sigma^2}\right\}$$

where, $x_0 = 12.5/2 = 6.25\text{GHz}$ and $\sigma = 5.31\text{GHz}$ for the AWG used. The AWG crossover optical frequency was thermally controlled to $f(0) = 193.1\text{THz}$, and the

3 Demonstration of automatic phase-locking operation

We examined the automatic pull-in and phase-lock operation of our proposal. The LD used was an external-cavity-structured LD (E-LD) identical to the one used in Ref. 6. Its FM response is $-20\text{MHz/mA}$ to $-2.8\text{MHz/mA}$ between DC and $1\text{MHz}$, as shown in Fig. 2(a). The optical frequency pull-in operation was monitored by utilizing our optical frequency discrimination circuit that had been developed for $20\text{Gb/s}$ QPSK homodyne detection, see Ref. 6, as shown in Fig. 2(b). The optical frequency discrimination circuit is comprised of a $12.5\text{GHz}$-spaced arrayed-waveguide grating (AWG), two pin-photodiodes followed by trans-impedance amplifiers and a differential amplifier. The set of electrical amplifiers forms a balanced amplifier that exhibits a common-mode rejection ratio (CMRR) of over $43\text{dB}$ for a measurement bandwidth between DC to $10\text{MHz}$. The AWG’s transmittance has a Gaussian profile of

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transmittance of two adjacent ports separated by 12.5 GHz (3 dB down) is as shown in Ref. 6. The discrimination sensitivity at crossover frequency was 1.4 MHz/mV for AWG input optical power of 6.0 dBm. The circuit output voltage for a frequency shifts of 100 MHz was 71 mV. Note that the common mode amplitude component, triggered by the injection current variation, was completely suppressed due to the circuit’s CMRR and we could extract the true optical frequency behavior of the light emitted by the LD.

Before processing the BSA, we set the LD optical frequency at about ±100 MHz from \( f(0) \) of OFCR by monitoring the beat frequency. After frequency setup, the phase-lock loop was turned on and confirmed automatic pull-in and phase-lock operation. The results are shown in Fig. 2(b) and (c).

**Fig. 2.** Measurement results for pull-in operation.

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**Fig. 3.** Measured RF spectrum and SSB phase noise.
When $f_{\text{beat}}$ was set at $-100$ MHz from the reference microwave frequency of 400 MHz (see the inset spectrum of Fig. 2(b)), the discriminator output showed that the optical frequency automatically shifted from $-100$ MHz to 0 in 0.45 ms. Setting $f_{\text{beat}}$ at $+100$ MHz, as shown in Fig. 2(c), the optical frequency shifted from 100 MHz to 0 in 0.28 ms. After transition, we confirmed the phase-lock state by observing the RF spectrum. The measured RF spectrum and SSB phase noise are shown in Fig. 3(a) and (b), respectively. We can see 60 dB beat note power to noise level at around the center frequency (= 400 MHz) and a smooth noise floor spreading to 3 MHz. This noise floor indicates a 3 MHz PLL bandwidth. Note that the spur at 0.5 MHz offset frequency observed in the beat spectrum is crosstalk from the digital thermo controller for E-LD. SSB phase noise has a standard deviation of only 1.6° and 1.8° for offset frequencies from 10 Hz to 3 MHz and 5 MHz, respectively (Agilent Technologies: N9010A), as shown in Fig. 3(b).

These results confirm that our developed MA-PLL circuit achieves automatic pull-in and phase-lock operation.

4 Conclusions

We successfully demonstrated signal light carrier automatic pull-in and phase-lock operation by our newly developed microcomputer-assisted phase-lock loop circuit. It achieves automatic phase-lock within 0.45 ms when the laser-diode frequency lies within the pull-in range of $\pm100$ MHz. The achieved phase-lock state exhibited SSB phase noise of just 1.8° at 5 MHz offset frequency.

Acknowledgments

The work is partly supported by National Institute of Information and Communication Technology (NICT) Japan and JSPS KAKENHI Grant Number 15H04009.