Room temperature wafer bonding is regarded as an enabling technology for micro electro mechanical systems (MEMS) and microfluidic devices packaging. Since bonding process is often the last step of packaging processes for MEMS devices, high temperature processing for bonding is not possible at that stage because of thermal mismatch problems and gas formation in the cavities that degrade device performance. MEMS devices are interfaced with real world systems and responded to incoming signals. In addition, many MEMS devices such as resonators, accelerometers, etc. require hermetic vacuum sealing or controllable cavity pressure in order to protect them from harsh environments, internal gases, mechanical damage, and contaminations. Furthermore, it is well known that the packaging cost is about 80% of the total fabrication cost for devices, which can be reduced by wafer-level packaging. So there is a significant and persistent demand for low temperature wafer-level bonding techniques for MEMS packaging. On the other hand, fabrication of microfluidic devices (for microparticles detection and counting and identification of microparticle types using fluorescence and blood cell analysis) is being performed either adhesive layer bonding, or high temperature bonding (1000-1200 K). Solvent extraction and analyte adsorption, and channel distortion are major issues in the adhesive and the high temperature bonding, respectively. In order to get rid of packaging issues of MEMS and microfluidics devices, we have developed a room temperature wafer bonding technique called surface activated bonding (SAB) process. The SAB is a solid-state bonding process that joins two similar or dissimilar smooth surfaces cleaned by an Ar-fast atom beam (Ar-FAB), an Ar-ion beam or a rf plasma beam in high vacuum/ultra high vacuum at room temperature due to the atomic forces of mating surfaces. The article briefly reports on the bonding results of bare and patterned Si/Si, Si/Glass, and Glass/Glass wafers containing MEMS devices and micro-fluidic V-groups by a low energy Ar-ion beam in high vacuum at room temperature.

Mirror polished single crystalline silicon (100) and (110) wafers were used for the fabrication of cavities for vacuum seal test and microfluidic devices, respectively. The diameters of wafers were 200- and 100-mm with the respective thicknesses of 730- and 200-μm. A 2-μm thick tetraethoxysilane (TEOS) film of pure silica was deposited on Si wafer surface by pressure-chemical vapor deposition method followed by photo resist coating and patterning (by a stepper). The cavity structures were fabricated by the deep reactive ion etching. Finally the wafers were cleaned by standard cleaning process.

We have loaded the bare and patterned Si wafers into the load lock chamber and then sputtered separately in the processing chamber by a hollow cathode low energy argon ion source (Mark II, Commonwealth Scientific Corp.) at an incident angle of 90° with a voltage of 80 V and an amperage of 3 A, for 30-180 s. The top sample was turned over in the turning over and pre-alignment chamber and then transferred to the alignment and pre-bonding chamber. The bottom sample was directly transferred to the alignment and pre-bonding chamber after being sputtered in the processing chamber. Preliminary bonding was performed in the alignment and pre-bonding chamber under a load of 500 N. Figure 1 shows the schematic diagram of the SAB tool used for the bonding experiments.

![Fig. 1. Schematic diagram of the wafer level SAB tool.](image)

Figure 2-5 show a few typical paradigms of bare Si/bare Si, bare Si/structured Si, bare Si/Si with micro-fluidic cavities, and fracture images of bare Si bonded with Si having micro-fluidic cavities, respectively. For micro-fluidic cavities, there are 180 cavities in one cell fabricated on 200-mm thick Si wafer. Each cavity is 11.5 mm long, 180-μm deep and 20-μm wide. White area is the bonding region and black area is the non-bonding region. Infra-red (IR) images show that there are no significant voids across the interface of Si/Si wafers with
(Fig. 2) and without (Fig. 3, right side) fine patterns. Fracture images evident bulk fractures both in bare and patterned regions. In addition, the estimated interface strength for Si/Si and glass/glass ranging from 10-20 MPa was comparable to the strength of bulk materials. However, radiation induced amorphous layer at the Si/Si interface is found, which is indicative of distorted short range order of Si atoms. We have further measured the leak rate of the Si/Si cavities and the results show that the leak rate of the cavities is $2.6 \times 10^{-16}$ Pa m$^{-2}$/s, indicating vacuum tight cavities. Chemical reliability of the Si/Si interfaces processed by low energy activation compared with plasma activation will also be presented.

Fig. 2. Infrared image (IR) of two 200-mm Si interface bonded at room temperature (RT).

Fig. 3. Bare and structured 200-mm Si wafers bonded at RT. Peripheral de-laminated area is due to wet etching caused surface damage.

Fig. 4. IR image for microfluidic cavities formed by bonded 4 inch Si wafer at RT.
Two cavities out of 180 cavities in one cell are shown on the right side with high magnification.

Fig. 5. Fracture images of microfluidic cavities by bonding between 200 and 100-mm Si wafers at RT. Bulk fracture through the bonded space between the cavities is evident.