1. Introduction:

Recently, the increased markets on wireless communications and automobiles require packaging various functional LSI-chips and MEMS components, which are produced in incompatible processes. For that reason, hetero-integrated packaging (HiP) technology was believed as a promising board level integration that can integrate MEMS devices and LSI chips by lateral interconnections (Fig.1) or micro-bumps, known as face-up or face-down types, respectively. In the present work, we aim at developing Cu lateral interconnections over Si-chip with a thickness of 100 um. However, the large height differences between chip and supporting wafer always cause problems, such as difficulties of transferring mask pattern to sample due to different depth-of-fields in photolithography and low coverage of each layer on chip lateral side. These problems of high topography step were often reported in the process of forming micro parts in MEMS. In the present work, we employed a mask aligner with a thick photoresist and Cu electroplating for the formation of high-step-coverage lateral interconnections extending over chip.

2. Experimental:

The experiment steps are illustrated in Fig. 2:
(a) Thermal oxidation of Si wafer (SiO2: 100 nm)
(b) Dry etching a 10 um step.
(c) Self-assembly of Si-chips (~100 um). [Ref.(1), (2)]

Fig. 1 Schematics of (a) MCM module and (b) the hetero-integrated packaging (HiP) technology.

Fig. 2 Experiment process flow.
3. Results and discussions:

Fig. 3 shows cross-sectional view of thick photoresist spin-coated on a 100-um-thick chip. The thickness of the photoresist at the top of the chip was 20 um. It has an acceptable coverage at the edge and the corner of Si-step after spin-coating and soft bake.

Fig. 6 SEM images of lateral interconnections.

Lithography results are shown in Fig.4, where the original sizes of mask line pattern are 4 um, 8 um, 16 um and 32 um. Exposure dose over 3000 mJ/cm² (typical mercury lamp, I-line) was adequate to sensitize photoresist at the bottom corner of Si-chip. However, SEM images shown in Fig. 5 reveal the sizes of Cu interconnections, against the original mask line widths, widen to 36 um, 50 um, 75 um and 100 um respectively.

Moreover, it’s found that, the widths of fabricated interconnections are also spatially different. As seen in Fig.5a, line widths on chip surface and bottom corner of Si-chip are 36 um and 25 um, respectively. The reason can be interpreted as the photoresist thickness differences, as seen in Fig. 3b.

Fig. 6 shows SEM cross-sectional views of the proposed Cu interconnection structure (a) extending from wafer up to chip surface, (b) on chip surface, (c) Si-chip bottom corner and (d) upper corner of Si-chip. The coverage ratios (thickness on surface divides those on chip lateral side) for each formed layer are, 3:1, 3:1, 1.5:1, 1:1 for Ta barrier layer, Cu seed layer, Plasma CVD SiO2 layer and Cu electroplating layer.

4. Conclusions:

High-step-coverage Cu lateral interconnections extending over Si-chip was successfully fabricated. The existing high topography step was demonstrated having small influence on the coverage of Cu lateral interconnections.

5. References:


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