Selectively formed GaAs quantum nanostructures and their application to single electron integrated circuits*

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We propose and fabricate a 1-bit adder circuit having only two single electron transistors (SETs) for AND and XOR logic operations by using SA-MOVPE. Two SETs have two common input gates and different Coulomb oscillation periods. The logic operation can be achieved on the basis of a binary decision diagram (BDD) architecture using Coulomb blockade (CB) in GaAs dots. We also demonstrate Coulomb oscillations caused by input gate voltages for a SET. Oscillation features of two input gates are the same and their phases can be shifted by the control gate. [DOI: 10.1380/ejssnt.2006.180]

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I. INTRODUCTION

The single electron transistor (SET) potential for ultra-low power consumption and highly functional features is very promising for use in future large scale integrated logic circuits (LSIs). This is because SETs can control the number of electrons in a nanoscale island via Coulomb blockade (CB) effects [1–6]. For a single electron logic system, a new architecture, that is, a binary decision diagram (BDD)-based architecture has been used instead of a conventional architecture for current LSIs because of the practical problems with SETs. Those problems include small gain and the unilateral nature of the devices [7–12]. In this architecture, a unit element of the circuit is called a BDD node device, which works as a path switch of single electron transport between two branches using Coulomb blockade effect. In this way, any complicated logic function can be achieved through the combination of node devices.

To develop SETs and their circuits, fabricating nanometer-scale electron channels having quantum dots with tunneling barriers, load resistance, and input/output electrodes is important. Selective-area metalorganic vapor phase epitaxy (SA-MOVPE) is one of the most promising fabrication methods due to its excellent ability to control position and size [13]. SA-MOVPE technology allows us to fabricate various kinds of semiconductor quantum nanostructures and their dense arrays only with one-step growth by using an appropriate mask designing of the substrate. Therefore, developing integrated circuits based on nanostructures and single electron devices is possible.

In previous papers, we reported on the fabrication and experimental operation of SET logic circuits based on networks of GaAs quantum dots and wires. Arrays of SETs utilizing quantum dots are fabricated by using SA-MOVPE on partially masked GaAs substrates. Based on these nanostructures, a single electron AND/NAND

circuit and a 1-bit adder circuit using BDD logic architecture was fabricated by integrating four and three SETs, respectively [3, 12]. In this study, we propose and fabricate a 1-bit adder circuit using only two SETs that function as an AND and an exclusive OR (XOR) logic circuits. The basic operation mode of each SET is partly demonstrated.

II. DEVICE DESIGN

First, we propose a BDD-based a 1-bit adder circuit consisting of two SETs that correspond to XOR and AND logic circuits. In Fig. 1(a), an equivalent circuit of a 1-bit BDD adder is shown. Two triple-gate SETs are integrated in this circuit, which consists of three ohmic pads, two control gates (CG1, CG2), and two main gates (MG1, MG2). Each control gate is used to form the quantum dot and tunneling barriers as well as to tune the phase of Coulomb oscillations. Main gates correspond to the input for the 1-bit adder. Three ohmic pads correspond to 'root', 'AND', and 'XOR' terminals.

The operation principle of this circuit as a BDD 1-bit adder is as follows. In Fig. 1(b), the logic table of a 1-bit adder and the XOR and AND operations using triple-gate SETs is shown schematically. A SET for the AND operation is configured to have a smaller dot capacitance than that of the XOR operation, which means that the Coulomb oscillation period for AND is longer than that of XOR. To achieve this condition, the input voltages of the three gates for the two SETs are adjusted appropriately. On the XOR side, when only one of the gates corresponds to the logic input '1', the current output is on a Coulomb oscillation peak. For the other inputs, current output is in a Coulomb blockade state [13]. On the AND side, when both inputs are set to 1, current output is on a Coulomb oscillation peak. On the other hand, for the other combinations of gate inputs, current output is in a Coulomb blockade state. In this circuit, using an additional control gate (third gate) for adjusting the Coulomb oscillation phase is necessary because adjusting the output by means of 'Coulomb blockade' or 'Coulomb peak' only by choosing two common input gate voltages is difficult. As a result, one SET operates as the AND circuit and the other operates as the XOR circuit, and the whole circuit

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FIG. 1: (a) Equivalent circuit of 1-bit BDD adder. (b) Logic table of 1-bit adder and the operation principle of BDD XOR SET and AND SET to total input.

FIG. 2: (a) Schematic illustration of the mask pattern on the GaAs substrate for a SET. (b) Schematic illustration of the SET after the growth and grown layer structure.

is expected to work as a 1-bit adder circuit.

In a previous report, we successfully demonstrated a 1-bit adder circuit integrating three SETs, in which the AND operation was achieved using two SETs [12]. To further decrease the number of transistors, we proposed a 1-bit adder integrating two SETs with different Coulomb oscillation periods. In a CMOS logic circuit, we typically need 14 transistors (ten transistors for XOR and four transistors for AND) to form a 1-bit adder. The number of transistors of this adder is significantly less than typical CMOS 1-bit adders.

III. EXPERIMENTAL RESULT AND DISCUSSION

To fabricate SETs, AlGaAs/GaAs modulation doped double heterostructures were grown by using SA-MOVPE on GaAs (001) substrates partially masked with a zig-zag opening area. Figure 2(a) is a schematic of the mask pattern on the GaAs substrate for a SET. A 40 nm thick SiON mask was used in SA-MOVPE. The mask pattern was formed by electron beam lithography and wet chemical etching (BHF;HF(48%):NH₄F (40%):H₂O

FIG. 3: Scanning electron microscope (SEM) image of GaAs 1-bit BDD adder.

= 1:10:100). SA-MOVPE growth was carried out using low-pressure horizontal, RF-heated, quartz reactor systems. A working pressure of 76 Torr was automatically controlled. Purified hydrogen (H_2) was used as a carrier gas. Trimethylgallium (TMGa), trimethylaluminum (TMAI), and 20% arsine (AsH_3) were used as the source materials. The partial pressures of TMGa and TMAI were maintained at 3.8×10^{-6} and 6.3×10^{-7} atm, respectively. The partial pressures of AsH_3 were maintained at 1.3×10^{-4} atm for the GaAs buffer layer, and 6.7×10^{-4} atm for the $Al_{0.3}Ga_{0.7}As$ layer to achieve a better quality. The growth rate of GaAs was $0.94 \mu m/h$, and that of $Al_{0.3}Ga_{0.7}As$ was $1.13 \mu m/h$ for planar substrates, respectively. The growth temperature was $700^\circ C$. Figure 2(b) is a schematic of the SET in which the grown layer structure is shown. Typical mobility and carrier concentration of a two dimensional electron gas (2DEG) formed on a reference planar substrate were $20,200 \text{ cm}^2/Vs$ and $5.6 \times 10^{11} \text{ cm}^{-2}$ at 77K, respectively. After the growth, first, Ge/Au/Ni/Au (50/100/25/100 nm) ohmic contacts were formed at the source and drain by the lift-off technique. Next, Schottky contacts for gates to control the 2DEG channel were formed by Cr/Au (10/15 nm) using the lift-off technique.

The GaAs channel width was smaller than the lithographically defined width on the substrate because of the appearance of inclined facets during crystal growth. The channel width was modulated through the zigzag-shaped mask pattern and sidewall facet, and it was squeezed especially at the two constrictions as shown in Fig. 2(b). When the negative control gate voltage was supplied, two tunneling barriers were formed at these positions. Thus, the SET structure was formed through the combination

FIG. 4: (a) and (b) Typical I_d - V_G characteristics measured for SET on left in Fig. 3. (c) Coulomb peak shift caused by the control gate voltage.

of a self-organized structure formed during crystal growth and lithographically defined gates. The transport properties of SETs and circuit operations were measured at low temperature.

In Fig. 3, a scanning electron microscope (SEM) image of a GaAs 1-bit BDD adder is shown. Two triple-gate SETs are integrated in this circuit, which consists of three

ohmic pads, two control gates, and two main gates. That is the same as the equivalent circuit shown in Fig. 1(a). Each control gate is used to form the quantum dot and tunneling barriers and to tune the phase of Coulomb oscillations. Details of the fabrication process were already reported elsewhere [14].

In Figs. 4(a) and 4(b), typical I_d - V_G characteristics measured for the SET on the left side in Fig. 3 under a constant source-drain voltage of 0.1 mV at 1.8 K are shown. The Coulomb oscillations were observed by each main gate. Oscillation periods obtained by applying gate voltages were almost the same for these two main gates because their gate capacitances are equal. Furthermore, the Coulomb peak was linearly shifted by the control gate voltage, as shown in Fig 4(c). This indicates that the phase of the Coulomb oscillations can be controlled by the control gate.

These results suggest that 1-bit adder operation using two SETs, which operate single electron BDD XOR and AND logic, is possible. However, an additional two side gates are needed to adjust the voltage swing of the main gate between two SETs to change their on/off status. The next step is to integrate two SETs with different Coulomb oscillation periods. The most promising method is the formation of an asymmetric common main gate on two SETs to have different gate capacitance.

The advantage of the present logic circuit using a multiple-gate SET and BDD architecture is that fewer transistors are needed than those of CMOS logic. In addition, power consumption is lower. The low gain of BDD logic circuits is another important problem for large-scale integration. For practical use, transistors to amplify the logic output signal to drive the next BDD logic must be in-

tegrated somewhere in a large-scale integration of a BDD logic circuit.

We will consider the operating temperature of SETs. Our present SET circuits operate only under very low temperature because the effective dot diameter of the present SET is about 60 nm. Further optimization of the fabrication process, especially crystal growth conditions, should reduce the dot diameter to as short as 10 nm and increase the operating temperature to 77 K.

IV. CONCLUSIONS

We proposed and fabricated a 1-bit adder circuit using only two SETs for AND and XOR logic operations. Two SETs had two common input gates and different Coulomb oscillation phases. The logic operation can be achieved based on a BDD architecture using Coulomb blockade (CB) in GaAs dots. Their transport properties were also investigated at low temperature. Coulomb oscillations were observed in SET transport measurements, and the Coulomb peak was found to shift by the control gate voltage. It is expected to operate as a 1-bit BDD adder after further optimization of the fabrication process and device parameters.

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