National Project on 45 to 32 nm Metal Oxide Semiconductor Field Effect Transistors for Next Century IC Fabrications*

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(Received 16 June 2008; Accepted 24 December 2008; Published 4 April 2009)

It is well known that the Taiwan Semiconductor industries play the very key roles for the worldwide IC foundry, and the advanced research of nanoelectronics is the lifeline for its long term developments. Professor Huey-liang Hwang effectively integrated the most outstanding research team and resource in Taiwan on the National Project on Nanometer CMOS Transistors for the 21 century, which is sponsored by the Ministry of Economic Affairs of ROC. A dozen of Professors from NTHU (National Tsing Hua University) with expertise at the novel materials and analysis and research at NCTU (National Chiao Tung University) with expertise at devices and reliability are devoted to the studies and are in collaboration with the world-wide-known company such as TSMC, and breakthrough of the key technologies of 45-32 nm technologies are achieved. The objective of this project is focused on the development of advanced metal gate/high-k MOSFET for 45 nm node generation and beyond, the efforts include the thermal stability of HfO₂, HfAlOₓ alloy and Al₂O₃/HfO₂ stack, prepared by ALD were compared, the incorporation of Al in alloy form gave superior characteristics by retaining an amorphous structure up to 1000°C, which suppress the leakage current and retards growth of the interfacial layer giving the least increment of EOT and interface traps. Besides, by incorporating Al into TiO₂ gave an EOT value of the Al₂O₃/TiAlOₓ/Al₂O₃ film down to 0.8 nm. Furthermore, high selectivity was obtained via etching the HfAlO and silicon wafer with pattern using the ICP Plasma. In this project, YbSi metal gate for n-MOSFET and IrSi metal gate p-MOSFET were successfully fabricated for the HfAlON MESFET. The results showed the good effective workfunction of 4.15 and 4.9 eV and no degradation of gate dielectric current and mobility in the YbSi/HfAlON and IrSi/HfAlON FUSI-gates by reducing the metal diffusion at lower temperatures. [DOI: 10.1380/ejssnt.2009.507]

Keywords: Metal gate; High-k; Gate dielectric; MOSFET; Interfacial layer; Work function

I. INTRODUCTION

Many high-k materials are currently considered as potential replacements of SiO₂ for gate dielectrics in future complementary metal-oxide-semiconductor (CMOS) technology [1–7]. Among the high-k candidates, HfO₂ has attracted much attention due to its higher dielectric constant (k =20-25) and relatively large band gap (E_g ~5.6 eV) [8–10]. However, the HfO₂ suffers from poor thermal stability, low crystallization temperature and high oxygen diffusivity through the thin films. These disadvantages would limit its application in the CMOS devices. In contrast, Al₂O₃, the other candidate having a relatively lower dielectric constant, can remain amorphous up to 1000°C and is known to have a much lower oxygen-diffusion coefficient compared to HfO₂ [11]. In addition, the Al₂O₃ has a large band gap of 8.8 eV and large band offset, which are helpful to reduce the tunneling leakage current. Many studies have been focused on the HfO₂ incorporation with aluminum in the form of HfAlOₓ alloy [12–14] or Al₂O₃/HfO₂ stack structure [15–17] as the gate dielectric to improve the thermal stability of HfO₂ thin films. However, the study on the effect of Al incorporation in these two different kinds of oxide structure has not been comparatively investigated in detail.

The quality and extent of charge trapping in the interfacial layer between high-k dielectric and silicon have been...
II. EXPERIMENTAL

The HfO$_2$, HfAlO$_x$ alloy and Al$_2$O$_3$/HfO$_2$ stack were deposited by ALD method at 200°C on p-type (100) Si substrate. The Si wafers were cleaned by standard RCA process and dipped with dilute HF solution to remove the native oxide before the deposition of high-k dielectrics. Trimethyl aluminum [TMA, Al(CH$_3$)$_3$], tetrakis (ethylmethylamino) hafnium [TEMAH, Hf[N((C$_2$H$_5$)CH$_3$)$_4$], and water (H$_2$O) were used as precursors, and argon was employed as carrier and purge gas. Three different kinds of samples were deposited for totally 40 cycles in sequence of 40H for HfO$_2$, (1A2H)*13+1A for HfAlO$_x$ alloy and 14A/26H for Al$_2$O$_3$/HfO$_2$ stack, where the “H” refers to one HfO$_2$ cycle and “A” one Al$_2$O$_3$ cycle. The cycle ratio of H/A was the same for alloy and stack structure to maintain the same Hf/Al composition ratio. After oxide deposition, all the samples were annealed by RTA (rapid thermal anneal) for 30 s in nitrogen atmosphere at different temperatures to improve the oxide quality and then changed to forming-gas atmosphere at 300°C for 30 mins to improve the interface quality.

reported to strongly affect the electrical characteristics of high-k MOS devices [18]. Some reports have proposed an charge-pumping (CP) extraction method to evaluate the depth profile of border traps situated in the gate oxide of MOS device [19]. However, only few studies have been reported on measuring the spatial distribution of bulk traps in metal-oxide-semiconductor field-effect-transistor (MOSFET) with high-k gate dielectric by CP technique.

Therefore, in this work, the gate dielectrics of HfO$_2$, HfAlO$_x$ alloy and Al$_2$O$_3$/HfO$_2$ stack were prepared on p-type Si (100) substrate by atomic layer deposition (ALD), and the thermal stability in relation to structural and electrical properties of the respective gate dielectrics in MOS structure were simultaneously studied.

FIG. 2: Mobility of Yb$_x$Si-Ir$_x$Si FUSI dual gates on HfAlON.

FIG. 3: The (a) C-V and (b) J-V characteristics of the HfO$_2$ thin films treated in N$_2$ plasma for different process times.

FIG. 4: The (a) C-V and (b) J-V characteristics of the HfAlO$_x$ gate dielectrics treated by different plasma nitridation process, PDA and high temperature process.
III. RESULTS AND DISCUSSION

A. Formation of metal-gate/high-k gate dielectrics in MOS devices

Figure 1 shows the $V_{fb}$ and EOT plot from measured C-V characteristics. The proper work function of 4.15 and 4.9 eV were obtained for Yb$_2$Si-Ir$_x$Si FUSI dual gates on HfAlON gate dielectric respectively, at 1.7 nm equivalent oxide thickness (EOT).

Figure 2 shows the field-effect mobility as a function of effective field. These metal-gate/high-k p- and n-MOSFETs show peak mobility of 80 and 180 cm$^2$/V·s, respectively.

B. Thermal stability enhancement of high-k dielectric in MOS devices by plasma nitridation

As demonstrated in Fig. 3(a), for as deposited HfO$_2$ (by the ALD system, without nitridation), C-V characteristic has an obvious difference after high temperature process (in N$_2$ gas at 900°C for 30 sec). It means that as deposited HfO$_2$ samples could not withstand the high temperature process. On the other hand, there is little difference in C-V characteristics for samples nitrided with N$_2$ plasma nitridation and the post-nitridation annealing (PNA), the C-V characteristic is less sensitive to the high temperature process. So it seems that the thermal stability of the HfAlO$_x$ thin films could be improved with the nitridation process, too. The J-V characteristic is presented in Fig. 4(b).

The plasma nitridation could be used to improve the thermal stability of HfO$_2$ thin films to bear a high temperature process at 850°C for at least 30 sec and the thermal stability of HfAlO$_x$ thin films to bear the high temperature process at 900°C for at least 30 sec.

C. Effects of bias power and pressure on etching rate of HfAlO and HfO$_2$ by BCl$_3$ plasmas

To study bias power effects, some Plasma parameters are fixed, such as ICP power: 500 W, Pressure: 10 mTorr, Gas: BCl$_3$/Ar (40/2 sccm), and Etch time: 60 sec.

As shown in Fig. 5, etch rates increase with increasing ICP power. It is also found that the etch rates of HfO$_2$...
are higher than those of HfAlO, which may be because the Al-O bonding is more strong than Hf-O one.

To study pressure effects, some Plasma parameters are fixed, such as ICP power: 500 W, Bias power: 10 W, Gas: BCl₃/Ar (40/2 sccm), and Etch time: 60 sec.

It observed in Fig. 6 that etch rate of HfAlO is lower than that of HfO₂ at 5 mTorr. The different etch rates between HfAlO and HfO₂ at various pressures suggest different etching mechanisms.

D. Comparison of stress-induced interface and bulk traps in high-k gated MOS devices

Figure 7 shows charge pumping current $I_{cp}$ of (a) HfO₂ and (b) HfZrO gated MOS devices under FN stress at $V_g = 1.3$ V as extracted from the charge-pumping data shown in Fig. 3.

The $D_{it}$ values of initial, after 500 s-stress, after 1000 s-stress for HfO₂ sample are $1.1 \times 10^{12}$, $9.4 \times 10^{11}$, and $8.5 \times 10^{11}$/eV·cm², respectively. The $D_{it}$ values for initial, after 500 s-stress, after 1000 s-stress for HfZrO sample are $3.1 \times 10^{11}$, $2.7 \times 10^{11}$, and $2.6 \times 10^{11}$/eV·cm², respectively.

Approximate depth profiles of border traps $N_{bt}(x)$ can be obtained by adopting the derivative $dQ_{cp}/d\log(f)$ [20]. Figure 8 shows bulk traps near interface $N_{bt}$ of (a) HfO₂ and (b) HfZrO gated MOS devices under FN stress at

FIG. 8: Depth profiles of border traps in (a)HfO₂ and (b)HfZrO gated MOS devices under FN stress at $V_g = 1.3$ V as extracted from the charge-pumping data shown in Fig. 3.

FIG. 9: Characteristics of $J$-$E$ plots for HfO₂ MOS at various temperatures.

$V_g = 1.3$ V measured at initial, after 500 and 1000 sec. Stress-induced bulk trap generation for both HfO₂ and HfZrO samples are clear. For HfZrO sample, the trap generation is saturated after 500s stress.

E. Current conduction mechanisms in high-k gate dielectrics

As gate oxide thickness is thinning down rapidly, unacceptable gate leakage current is an important reason for switching from conventional SiO₂ to high-k gate dielectrics. Therefore, current conduction mechanisms in high-k gate dielectrics are necessary to be understood. Figure 9 shows gate current density versus applied electric field ($J$-$E$) characteristics in the temperature range from 300 K to 550 K.

After analyzing the experimental data, it is found that the main current conduction mechanism should be Schottky emission. To elucidate this, a brief review of the mechanism is provided as follows. It is well known that Schottky emission can be expressed as [21]

$$ J = A^*T^2 \exp \left[ -q\phi_B - \sqrt{qE/4\pi\varepsilon_0\varepsilon_r} \right] / kT, $$

where $J$ is current density, $A^*$ is effective Richardson constant and $A^* = 4\pi q(m^*)k^2/h^3 = 120(m^*/m_0)$, $T$ is absolute temperature, $q$ is electronic charge, $\phi_B$ is Schottky barrier height, $E$ is electric field, $k$ is Boltzmann’s constant, $h$ is Planck’s constant, $\varepsilon_r$ is dynamic dielectric constant, $\varepsilon_0$ is permittivity of free space, $m_0$ is free electron mass and $m^*$ is electron effective mass in HfO₂.

For standard Schottky emission, a plot of ln($J/T^2$) versus $E^{1/2}$ should be linear. The experimental data in the region of high temperature (475 K-550 K) and high electric field (2.75-3.8 MV/cm) fit the Schottky emission theory very well for gate injection as shown in Fig. 10. Moreover, the fitted dynamic dielectric constant in the standard Schottky plots is very close to 4.15, which is the square of the refractive index $n = 2.04$ [22]. The intercept of the Schottky plot with the vertical axis can be expressed as Eq. (2) and is a function of the barrier...
The barrier height at the Al/HfO₂ interface and the electron effective mass in HfO₂, respectively. The discrepancies in electron effective mass and barrier height [23–25] may be related to the thin film characteristics and imperfections of the HfO₂ gate dielectrics, as well as the influence of HfO₂/Si and HfO₂/metal interfaces on the gate current density in the devices. Moreover, according to our recent progress [26], an interfacial layer (IL) between HfO₂ and Si is not SiO₂ and the barrier heights to be discussed in this work are effective values which include the effects of the interfacial layers.

IV. SUMMARY AND OTHER RELATED WORK OF THIS PROJECT

Some achievements of this project include the thermal stability of HfO₂, HfAlO₂ alloy and Al₂O₃/HfO₂ stack, prepared by ALD were compared, the incorporation of Al in alloy form gave superior characteristics by retaining an amorphous structure up to 1000°C, which suppress the leakage current and retards growth of the interfacial layer giving the least increment of EOT and interface traps. Besides, by incorporating Al into TiO₂ gave an EOT value of the Al₂O₃/TiAlO₂/Al₂O₃ film down to 0.8 nm. Furthermore, high selectivity was obtained via etching the HfAlO and silicon wafer with pattern using the ICP Plasma. In this project, YbSi metal gate for n-MOSFET and IrSi metal gate p-MOSFET were successfully fabricated for the HfAlON MESFET. The results showed the good effective workfunction of 4.15 and 4.9 eV and no degradation of gate dielectric current and mobility in the Yb₂Si/HfAlON and IrₓSi/HfAlON FUSI-gates by reducing the metal diffusion at lower temperatures.

Acknowledgments

The authors gratefully acknowledge the support from the Technology Development Program for Academia, Department of Industrial Technology, Ministry of Economic Affairs, Taiwan, Republic of China.
