Bias Stress and Memory Effect in Pentacene-based Organic Thin-Film Transistors with a Fullerene Layer

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Organic memory-transistor devices were fabricated from pentacene-based organic thin-film transistors (OTFTs) with a fullerene layer. The current-voltage (I-V) characteristics show that the fabricated OTFTs exhibit a unipolar property with p-channel characteristics. The fabricated OTFTs devices exhibit a threshold voltage shift upon the application of positive and negative bias. Under the effect of positive bias, the on state was induced and a $\Delta V_{th} = 12.9$ V was obtained. Meanwhile, the threshold voltage was reversibly shifted by $\Delta V_{th} = 9.1$ V under the effect of negative bias and the off state was induced. Upon the effect of bias, the carrier mobility of fabricated OTFTs is almost similar in both on and off states. Pentacene-based OTFTs without a fullerene layer for memory effect was demonstrated for comparison. The memory effect is mainly attributed to the fullerene layer.

[I. INTRODUCTION]

The research on organic semiconductors for their broad range of applications in semiconductor industry has attracted scientific and technological interest. Although electronic and semiconductor industry has been dominated by the impressive performance of inorganic semiconductors for many years, the attraction of using organic devices is driven by many advantages of organic semiconductors, including flexibility, simple structure, low fabrication cost, light weight, and solution processibility. There have been important developments in materials and device structures that enable us to expect in the near future the potential application of organic semiconductors [1]. Several types of organic devices have been proposed, including organic light emitting diodes, phototransistor, solar cells, and nonvolatile memory devices [2–6]. Among these organic devices, an organic memory device is still in the exploration stage although there is a clear demand for next generation of nonvolatile solid state memories [7]. These nonvolatile memory devices are essential component for integrated circuits (ICs) and system-on-chip (SOC) application based on organic thin-film transistors (OTFTs). The memory effect of these OTFTs devices occur upon the electrical effect [6, 8, 9] or photoresponse [10, 11] due to the charge or discharge of nanoparticles/nanocrystals in organic semiconductor layer. Memory effects often refer to charge-trapping effect where, programming by injecting charge and erasing by removing the stored charges. This charge transfer in the organic semiconductor layer is readable by measuring the shift of threshold voltage of the transistor [8, 10, 12]. Therefore, the unique properties of organic semiconductors allow the digital data to be programmed or erased through either electrically or optically.

In this paper, we introduce a new memory effect in devices consisting of all organic semiconductors that combine a bi-layer of pentacene and soluble fullerene. Specifically, we demonstrate memory effect of pentacene-based OTFTs with a fullerene layer upon the application of bias. These new devices are analogous to our previously reported organic memory devices, where charge storing carbon nanodots are embedded onto gate insulator incorporating pentacene as an active layer [12]. Previously, the devices had an issue of controlling the size of carbon nanodots. The advantages of incorporating fullerene is that fullerene molecules have a constant diameter and can be processed using solution based technique, creating a uniform layer. Thus, the advantages of using fullerene with pentacene will be significantly enhancing the storage density capability for future nonvolatile memory applications.

II. EXPERIMENT

A (100)-oriented Sb-doped $n^+$-type silicon wafer ($< 0.1 \Omega cm$) was cut into 1.5 cm×1.5 cm square chips as substrates, which were cleaned by ultrasonic cleaning in deionized water and methyl alcohol followed by a standard RCA cleaning procedure. Then, the $\text{SiO}_2$ gate oxide film was thermally grown in dry oxygen ambient at 1100$^\circ$C for 20 min to achieve a 40 nm thickness using a quartz furnace tube. Fullerene (soluble fullerene: PCBM) was dissolved in a common solvent dichloromethane at mass percentage of 0.3wt%. Fullerene layer was deposited on $\text{SiO}_2$ by a spin-coating method using a syringe with a fil-
FIG. 1: (a) Schematic diagram of pentacene-based OTFTs devices with a fullerene layer. (b) The chemical structure of (i) pentacene (Sigma Aldrich) and (ii) fullerene (soluble fullerene: PCBM) (Kanko Chemical). (c) AFM image of soluble fullerene (PCBM) layer surfaces.

ter of 0.2 μm in diameter. A 50-nm-thick pentacene layer was evaporated directly onto the top of the fullerene layer by vacuum evaporation at a deposition rate of 4 Å/sec under a pressure of 2.3×10−6 Torr. Au was evaporated on the organic bi-layer from tungsten coil through a designated shadow mask in vacuum chamber for top source and drain contacts (channel width, \( W = 2.5 \) mm and channel length, \( L = 50 \) μm). The schematic device structure is shown in Fig. 1(a). A control sample of OTFTs without the fullerene layer was also prepared for comparison. Finally, the electrical characteristics of fabricated OTFTs with and without a fullerene layer were measured in a shield box under atmospheric pressure at room temperature using a computer-controlled automatic electrical analyzer.

III. RESULT AND DISCUSSION

The chemical structure of the pentacene and the fullerene (soluble fullerene: PCBM) molecule are shown in Fig. 1(b). Figure 1(c) shows the atomic force microscope (AFM) image for the surface of the spin-coated soluble fullerene (PCBM). The AFM result indicates that the fullerenes were distributed and adhered on insulating layer.

Figure 2 shows the output characteristics \( (I_{ds}-V_{ds}) \) as a function of drain voltage \( (V_{ds}) \) with various gate voltage \( (V_g) \) for pentacene-based OTFTs with and without a fullerene layer. For both OTFT devices, as the \( V_g \) increased, the \( I_{ds} \) smoothly increased with applying \( V_{ds} \) (lower bias region, \( V_{ds} < -10 \) V). Comparing the output curves in the higher bias region \( (V_{ds} > -15 \) V), it was observed that the \( I_{ds} \) was perfectly saturated in both OTFTs. Both devices were exhibited typically \( p \)-channel transistor characteristics. Therefore, presence of fullerene layer did not affect the characteristic of pentacene-based OTFTs.

Figure 3 shows the transfer characteristics \( (I_{ds}-V_{ds}) \) as a function of gate voltage \( (V_g) \) at constant drain voltage \( (V_{ds} = -20 \) V). The transfer characteristics in saturation regime were measured to determine the threshold voltage \( (V_{th}) \) and the charge carrier mobility \( (\mu) \) of the OTFTs by employing conventional TFT equation [13]:

\[
I_{ds} = \frac{W \mu C_{ox}}{L} \left( V_g - V_{th} \right)^{2},
\]

where \( W \) is the channel width, \( L \) is the channel length, \( V_{th} \) is the threshold voltage, \( \mu \) is the charge carrier mobility, and \( C_{ox} \) is the capacitance per unit area of the insulating layer (SiO\(_2\)). The \( V_{th} \) was defined as the voltage at which the linear fit of the square-root of the drain cur-
FIG. 3: The $\sqrt{I_{ds}}$-$V_g$ characteristics for pentacene-based OTFTs (a) with a fullerene layer and (b) without a fullerene layer with a linear fit line to extract data for the threshold voltage and the charge carrier mobility. The inset in (a) and (b) show the transfer characteristics ($I_{ds}$-$V_g$) for both devices at $V_{ds} = -20$ V.

rent plotted versus the gate voltage ($\sqrt{I_{ds}-V_g}$) intercepts the gate voltage axis. The $V_{th}$ of the pentacene-based OTFTs with and without a fullerene layer were $-6.0$ V and $-10.2$ V, respectively. The $\mu$ of the OTFTs with a fullerene layer was $0.099$ cm$^2$/Vs calculated from the slope of the plot of $\sqrt{I_{ds}-V_g}$ as shown in the inset of Fig. 3(a). The $\mu$ of the OTFTs without a fullerene layer was $0.088$ cm$^2$/Vs obtained from the slope as shown in the inset of Fig. 3(b). The mobility of both OTFTs devices exhibits almost the similar value. However, our aim was not to improve the mobility of the devices but to investigate the memory effect occurring upon application of bias. Therefore, the fullerene layer between pentacene and insulating layer did not degrade the charge transport properties in the devices.

Figure 4 shows the transfer characteristic of pentacene-based OTFTs devices for memory effect application. The memory effect was carried out in which the transfer curves shifted before applying bias and after applying positive bias, and the transfer curves shifted reversibly to the origin after applying negative bias. The transfer characteristics of memory effect were carried out under three conditions; without bias, positive bias, and negative bias at a constant drain voltage of $-20$ V. In positive bias, $V_g = +5$ V was applied for 10 min, while in negative bias, $V_g = -5$ V was applied also for 10 min. The shift of transfer characteristic was determined by the value of threshold voltage shift ($\Delta V_{th}$). The transfer characteristic of pentacene-based OTFTs devices with a fullerene layer is shown in Fig. 4(a). At first, the transfer characteristic curve shifted in a positive direction when a positive bias was applied and in a negative direction after the application of a negative bias. Thus, the $V_{th}$ value was shifted reversibly by applying an appropriate bias. A $\Delta V_{th} = 12.9$ V was obtained after
a positive bias for 10 min and the on state was induced. This could be reversibly shifted with a $\Delta V_{th} = 9.1\, \text{V}$ after a negative bias, and the off state was induced. For comparison, Fig. 4(b) shows the transfer characteristic of pentacene-based OTFTs devices without a fullerene layer. However, only a little shift of threshold voltage was observed upon application of positive bias, but the threshold voltage cannot be shifted reversibly upon application of negative bias. Therefore, we confirmed that the on and off states (memory effect) was mainly owing to the presence of the fullerene layer between the pentacene layer and the insulating layer. We note that the gate voltage while measuring the transfer characteristics would also induce the $V_{th}$ shift. Due to the voltage sweep rate or the measurement time, the apparent threshold voltage can vary depending on the measurement conditions and the voltage history that the device experienced before measurement. The $V_{th}$ shift (hysteresis) is influenced by the value of the sweep rate [14]. Therefore, in order to minimize the threshold voltage variation, we used exactly the same condition (relatively quick voltage sweep rate of 164 mV/s) to measure our devices presented in Fig. 4. However, further improvement to the measurement technique is currently undergoing to get more information about the effects of sweep rate on the performance of our devices. In addition, the threshold voltages and the charge carrier mobilities in both devices were defined by the plot of $\sqrt{I_{ds}}$–$V_g$ (not shown) are summarized in Table I.

The shift of threshold voltage of several organic devices upon the application of bias stress has been suggested for nonvolatile memory effect owing to the charge-trapping effect [6, 8, 9, 15]. In these devices, applying a negative bias causes its $V_{th}$ to shift which related to an on state memory, while in applying a positive bias will erase the memory. Therefore, the mechanism of the $V_{th}$ shift in our devices is also similar to the others. In this work, positive bias induced positive $V_{th}$ shift. This can be explained by the introduction of the fullerene layer would slow down the electrons, and makes an easy path for holes to travel into pentacene. In the case that the device is set with a positive bias, electrons trapping to the PCBM islands are retarded, which causes more free holes are accumulated in pentacene, and hence the $V_{th}$ shifts to positive side as a result. When a negative bias is set to the device, electrons trapping are prevented and some trapped electrons at the PCBM islands are detrapped, which causes the recombination of trapped electrons with the free holes, and would be attributed to the decrease of free holes in the pentacene. As a result, the $V_{th}$ shifts to its initial position. Therefore, this indicates that for these on and off states, the fullerene layer is responsible for the shift of $V_{th}$ upon the application of bias. Thus, upon the application of bias between the gate and the organic semiconductor (pentacene/fullerene layer) channel could alter the charge carrier distribution in the devices. However, further investigation in the influence of fullerene layers towards the memory effect behavior, and physical properties between the pentacene-fullerene interfaces have to be examined by future study.

### IV. Conclusions

In brief, we have fabricated pentacene-based OTFTs with a fullerene layer. The electrical characteristics exhibited a unipolar property with strong $p$-channel characteristics. We have demonstrated that upon the application of bias in pentacene-based OTFTs devices with a fullerene layer manifest a positive threshold voltage shift for positive gate bias. The electrical characteristics exhibited a threshold voltage shift corresponding to a change of charge carrier distribution at the pentacene-fullerene interface, which confirmed the occurrence of a memory effect i.e., on and off states. Furthermore, the application of bias has no influence on the mobility. The use of soluble fullerene layer as the memory effect medium and an effective solution processable organic semiconductor is promising for nonvolatile memory effect application. Further studies are in progress to study the nonvolatile memory effect application with the on/off times, the cycling stability, and also to address the influence of fullerene layer on the memory effect performances.

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### References

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