Highly N-doped Silicon Nanowires as a Possible Alternative to Carbon for On-chip Electrochemical Capacitors

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ABSTRACT
Highly n-doped silicon nanowires (SiNWs) have been grown by a chemical vapor deposition process and have been investigated as possible electrodes for electrochemical capacitors (ECs) micro-devices. Their performances have been compared to existing literature on the field, which shows the use of SiNWs fabricated via different techniques, SiC coated SiNWs and porous silicon layers. The double layer capacitance of n-doped silicon wafer is \( \approx 6 \mu F cm^{-2} \) in standard organic electrolyte, and this value can be increased by nanostructuration of SiNWs up to \( 440 \mu F cm^{-2} \) by tuning deposition parameters. Similar values are found in the literature. Symmetrical microdevices based on two identical SiNWs electrodes can be operated in organic based electrolytes within a 1.2 V voltage window. The devices show excellent cycling efficiency over more than 2000 cycles, with capacitance value of \( 51 \mu F cm^{-2} \) and an energy density of \( 10 nWh cm^{-2} \). The increase of specific surface area by different techniques may drastically boost these values in the near future.

Keywords : Electrochemical Capacitor, Highly N-doped Silicon Nanowires, Micro-device

1. Introduction

Materials for electrochemical capacitors (ECs) so-called supercapacitors, are a growing field of interest since many applications are requiring fast rechargeable electrochemical devices which can last for more than 1,000,000 cycles. This is true for large scale devices such as Start & Stop system in cars, energy recovery devices implemented on harbor cranes or load-leveling systems in tramways & trains. There is also a need of energy storage systems in small integrated devices that can be operated with sensors, radio-frequency identification tags (RFIDs) or microelectromechanical systems (MEMS). Materials used in ECs can be divided in two categories, namely (i) those exhibiting electrochemical double layer capacitance and (ii) those exhibiting pseudocapacitive behavior. Electrochemical double layer capacitors (EDLCs) have a major advantage over pseudocapacitive materials which is the capacitive nature (major phenomenon) of charge storage. As a consequence, the surface of the electrodes is only poorly affected by charge accumulation which in turns provides very high cycling ability as well as high power capability.

Carbon is almost the only material envisioned as possible electrode for EDLCs, its capacitance being mainly driven by surface area, pore size distribution and interaction with electrolyte. Recently, silicon was evidenced as a possible EDLC material. Indeed, no faradic reaction seems to take place upon charging or discharging silicon based electrodes in various electrolytes. The main drawback of silicon is the difficulty to scale up the synthesis of high surface area material that can be used in large scale devices. Subsequently, most of the studies on silicon electrodes focused on the use of nanostructured silicon based electrodes in microdevices. This is probably where the use of silicon is meaningful since silicon nanostructures can be directly deposited on silicon wafer which are the primary bricks of microelectronic devices. This is also a field where silicon can directly compete with carbon as electrode material for EDLCs. Indeed, unlike silicon which can be directly grown on silicon substrate, carbon electrodes need to be provided through other means such as inkjet printing, even if some trials have been made in recent years to directly grow carbon electrodes on silicon wafer.

Silicon nanostructures, mostly silicon nanowires (SiNWs) have been used as substrates to deposit different electroactive materials such as NiO. In such case, the goal is to take advantage of the 1D nanostructure provided by SiNWs to provide a high surface expanding factor. EDLC electrodes based on SiNWs have also been characterized when coated with silicon carbide (SiC) or gold. However, a careful analysis of literature data only evidences few papers based on the use of pristine silicon as possible electrode in EC microdevices. This is the main topic of this paper which focuses on the growth of highly n-doped SiNWs (N-SiNWs) by different techniques, their electrochemical characterizations in standard organic based electrolytes and aqueous electrolytes, the key parameters to increase surface capacitance, as well as the comparison to existing literature on the field.

2. Experimental

2.1. Growth of SiNWs by chemical vapor deposition (CVD)
N-SiNWs were grown using our standard deposition process. A low-pressure CVD reactor (EasyTube3000 First Nano, a Division
of CVD Equipment Corporation) was operated at 600 or 650°C and 3 Torr total pressure. We used this temperature range for a good epitaxial growth with high growth rate (500–650 nm/min\(^1\)). Si(111) wafers were used as growth substrates and cleaned by dipping in acetone and isopropyl alcohol and de-oxidation in HF 10\%. Calibrated SiNWs were grown from gold colloids (BritishBioCell), with a 50–200 nm\(^\circ\). Alternatively, an evaporated thin gold film (4 nm) could be used as catalyst. Hydrogen (H\(_2\)) was used as the carrier gas (1.9 standard liters per minute), while silane (SiH\(_4\)) was used as the Si precursor (20–50 sccm, standard cubic centimeters, or 30–80 mTorr for SiH\(_4\) partial pressure). N-type doping was achieved by introducing PH\(_3\) into the reactor, with P\(_{PH3}\):P\(_{SiH4}\) ratio in the 10\(^{-6}\)–10\(^{-2}\) range. N-type doping level was estimated to \(N_d = 4.2 \times 10^{19} \text{ cm}^{-3}\) according to resistivity measurements in four probes configuration. Depending on the experiment, an additional HCl flux could be introduced into the reactor (0–100 sccm, or 0–160 mTorr HCl partial pressure) to avoid gold pouring along them. Thus, very long nanowires with similar diameters from the bottom to the top can be obtained. Scanning electron microscopy (SEM) images were obtained using a ZEISS ultrascan scanning electron microscope (SEM) equipped with an in lens secondary electron detector.

### 2.2 SiNWs electrochemical characterizations

All experiments were performed in a glove box at room temperature. The electrolyte was 1 M tetraethylammonium tetrafluoroborate (NEt\(_4\)BF\(_4\), FlukaChemika) in propylene carbonate (PC, Sigma Aldrich). Both n-doped silicon wafer and N-SiNWs grown by the different techniques were directly used as the electrode. The electrochemical characterization was carried out in 3 electrode set-up. The nanostructured side of the silicon is in contact with the electrolyte (S = 0.2 cm\(^2\)) while the back of the wafer is electronically connected to a stainless steel current collector. The reference electrode is an Ag/Ag\(^+\) electrode and the counter electrode a Pt wire.

For symmetrical device evaluation, N-SiNWs electrodes were assembled by clamping together two silicon electrodes (S = 1 cm\(^2\)) separated by a glass fiber paper impregnated with the electrolyte as separator. Electrochemical instruments consisted of potentiostat/galvanostat equipped with low current channels (VMP3 from Biologic monitored with EC-lab software).

### 3. Results and Discussion

#### 3.1 Microstructural characterizations SiNWs

Figure 1 compared N-SiNWs grown with different methods. Gold catalyst nanoparticles can be homogeneously dispersed at the surface of silicon wafer using two methods as depicted in Fig. 1(a). A 4 nm evaporated gold thin film (4 nm) could be used as catalyst. Hydrogen (H\(_2\)) was used as the carrier gas (1.9 standard liters per minute), while silane (SiH\(_4\)) was used as the Si precursor (20–50 sccm, standard cubic centimeters, or 30–80 mTorr for SiH\(_4\) partial pressure). N-type doping was achieved by introducing PH\(_3\) into the reactor, with P\(_{PH3}\):P\(_{SiH4}\) ratio in the 10\(^{-6}\)–10\(^{-2}\) range. N-type doping level was estimated to \(N_d = 4.2 \times 10^{19} \text{ cm}^{-3}\) according to resistivity measurements in four probes configuration. Depending on the experiment, an additional HCl flux could be introduced into the reactor (0–100 sccm, or 0–160 mTorr HCl partial pressure) to avoid gold pouring along them. Thus, very long nanowires with similar diameters from the bottom to the top can be obtained. Scanning electron microscopy (SEM) images were obtained using a ZEISS ultrascan scanning electron microscope (SEM) equipped with an in lens secondary electron detector.

#### 3.2 Other SiNWs

In the literature, different other techniques for growing SiNWs for EC applications are used. The SiNW arrays used as substrate for
Further SiC deposition is produced via wet etching of p-type Si(100) substrates (1–5 μm) using an oxidant etchant bath of 20 mM AgNO₃ and 5 M HF, respectively, at the bath temperature of 50°C. These conditions result in nanowires with a diameter range of 20–300 nm. SiC was then deposited onto SiNW arrays using a low-pressure chemical vapor deposition (LPCVD) reactor, employing methylsilane as the precursor and in situ doped using ammonia. The SiC NWs are grown by a Ni-catalyzed CVD process similar to that previously reported.

Another method consists in using stainless steel substrates with 50 nm gold layers deposited on top, and put them inside a quartz tube in a tube furnace. First, the substrates underwent a pre-growth step at 485°C for 30 min to break the gold film into nanoparticles. In the subsequent growth step, 2% silane (SiH₄) gas in argon is flown through the tube at 485°C for about 30 min at a rate of 50 sccm and constant pressure of 40 Torr. This growth process typically yields a SiNW mass of 0.5–1 mg cm⁻². The specific surface area measured by BET method is about 20 m² g⁻¹. However, the authors succeeded in expanding this surface area by a factor of 5 using a lithium insertion/removal pre-treatment in lithium based electrolyte. For this purpose, the SiNWs electrode was first cycled five times vs. metallic lithium as counter electrode and 1 M LiPF₆ in a 1:1 mixture of ethylene carbonate (EC) and diethyl carbonate (DEC) as electrolyte. Indeed such pre-treatment created a 1D porous nanostructure with uniform pore size distribution. There is no further indication whether the SiNWs are doped or not in order to improve electronic conductivity. The nanoporous SiNWs thus prepared are used directly as electrodes in EC micro-devices.

### 3.3 Porous silicon

Porous silicon (PSi) is a relatively high surface area material (600 m² cm⁻³ of actual material) which is produced by chemical or electrochemical etching of p- or n-type crystalline silicon. Electrochemical etching is the more commonly employed method as it is quicker and more reliable. The etching solution is usually a mixture of hydrofluoric acid (HF) in ethanol or water. The concentration of the etching solution together with the anodization current density and the etching time govern the properties of the PSi layer. These properties include the porosity (i.e. the percentage coverage of pores over the wafer surface), the shape and the depth of the pores.

For example, macroporous silicon electrodes (MPSi) can be made in a HF-H₂O solution added with a TritonX-100 surfactant from a p-type silicon wafer with a 30-50 μm resistivity and a (100) crystalline orientation. This material is known to allow the production of very well oriented macropores with diameters in the range of 1 to 5 μm. The electrodes are made by applying a constant current density of 58 mA cm⁻² on a silicon wafer as well as the dispersion of length and diameter of SiNWs. However, this demonstrates that the surface capacitance of n-doped silicon electrodes can be enhanced by growing N-SiNWs, in the same way as the capacitance of carbons can be increased by tuning their pore size distribution and their specific surface area. Further improvement in the surface capacitance can be made by increasing the length of nanowires as depicted in Fig. 2(c). While keeping the same diameter (50 nm), an increase from 5 up to 20 μm in the length of N-SiNWs also results in an increase by a factor of 4 of the capacitance (26 to 105 μF cm⁻²). The use of de-wetted gold nanolayer as catalyst significantly improves the density of N-SiNWs on the surface of silicon wafer, from 10⁴ up to 3 x 10⁵ NWs cm⁻². 5 μm thick N-SiNWs grown by this method exhibit a capacitance value of 106 μF cm⁻², which is equivalent to the capacitance of SiNWs 20 μm in length grown by gold colloids. Increasing the length of N-SiNWs (up to 50 μm) grown by de-wetted gold nanolayer leads to an even more disordered nanostructure. Due to the wider diameter distribution, to longer SiNWs, and to a higher density of N-SiNWs on the surface, a value of 440 μF cm⁻² is obtained.

The different capacitance values for SiNWs electrodes measured in 3 electrode cell configuration are summarized in Table 1. It is quite difficult to compare the values measured on N-SiNWs to existing literature. Probably due to the low intrinsic double layer
capacitance of silicon and to the use of poorly doped silicon, most of the authors have chosen not to use directly SiNWs as electrode but rather to use them as 1D substrates to grow other electrode materials on their surface: SiC, gold, or NiO. Moreover, the data on pristine silicon are only reported for devices and not for single electrode measurement in a standard 3 electrode cell. The only indication found in the literature about the investigation of SiNWs is that they are anodized at potentials above +0.4 V vs. Ag/AgCl in 1 M KCl aqueous electrolyte. Unlike SiNWs, silicon carbide nanowires (SiCNWs) can sustain long term cycling test in 3.5 M KCl aqueous electrolyte within a potential window of −0.2 to +0.6 V vs. Ag/AgCl. The effect of the 1D nanostructuration is easily demonstrated since 6 µm thick SiCNWs exhibit 38 times more capacitance (240 µF cm⁻²) than SiC thin film alone. It can be noted that the double layer capacitance (DLC) of SiC thin film is substantially lower (6 µF cm⁻²), which is the value measured for n-doped bulk Si wafer. Increasing the length of SiNWs to 32 µm leads to an increase of the capacitance up to 1700 µF cm⁻² (Table 1). Despite similar capacitance values for bulk materials, SiCNWs exhibit some superiority in terms of capacitance compared to SiNWs (Table 1). Indeed, 6 µm length SiCNWs show nearly 10 times more capacitance than 5 µm length SiNWs. Such higher capacitance can originate from two main differences: (i) SiCNWs were operated in aqueous electrolytes which usually provide higher double layer capacitance values than organic based electrolyte in which SiNWs were tested, and (ii) the synthesis methods differ significantly so that the surface enhancement factor might not be identical in all cases. Indeed, the etching of p-type silicon substrate leads to very dense layers of SiNWs that are further covered by SiC.

Thus it is possible to adapt the nanostructuration of SiNWs in order to improve the surface enhancement factor which in turn provides more surface capacitance to the electrode. Subsequently, symmetrical EC microdevices were assembled with our N-SiNWs and compared to similar devices shown in the literature.

### 3.5 Assembly of silicon based EC micro devices

The literature on silicon based micro-supercapacitors is more prolific than single electrode characterization. The second part of Table 1 summarized the different devices that have been assembled and evaluated.

The most amazing performance were reported for porous SiNWs prepared by the peculiar method described in Cui’s paper. The device assembled with two symmetrical pristine SiNWs exhibits a BET surface area of 20 m² g⁻¹ with a specific capacitance of 20 F g⁻¹. For a single electrode, the capacitance should be 4 × 20 F g⁻¹ = 80 F g⁻¹. This translates into a double layer capacitance of 400 µF cm⁻², which is 80 times higher than that measured for

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**Table 1. Summary of literature data on silicon based ECs.**

<table>
<thead>
<tr>
<th>Electrode material</th>
<th>Electrochemical</th>
<th>Electrolyte</th>
<th>Capacitance per substrate area (µF cm⁻²)</th>
<th>Energy density (nWh cm⁻²)</th>
<th>Number of cycles</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-Bulk Si</td>
<td>−0.5 to −1.3 V</td>
<td>1 M NEt₄BF₄</td>
<td>6</td>
<td>@ 50 mV/s</td>
<td>—</td>
<td>6</td>
</tr>
<tr>
<td>p-SiNWs (11 µm thick 100 nm)</td>
<td>−0.5 to −1.3 V</td>
<td>1 M NEt₄BF₄</td>
<td>48</td>
<td>@ 50 mV/s</td>
<td>—</td>
<td>6</td>
</tr>
<tr>
<td>SiNWs (5 µm thick 50 nm)</td>
<td>−0.4 to −1.2 V</td>
<td>1 M NEt₄BF₄</td>
<td>26</td>
<td>@ 50 mV/s</td>
<td>—</td>
<td>This study</td>
</tr>
<tr>
<td>SiNWs (20 µm thick 50 nm)</td>
<td>−0.4 to −1.2 V</td>
<td>1 M NEt₄BF₄</td>
<td>105</td>
<td>@ 50 mV/s</td>
<td>—</td>
<td>This study</td>
</tr>
<tr>
<td>SiNWs (50 µm thick 20−200 nm)</td>
<td>−0.4 to −1.2 V</td>
<td>1 M NEt₄BF₄</td>
<td>440</td>
<td>@ 50 mV/s</td>
<td>—</td>
<td>This study</td>
</tr>
<tr>
<td>SiC/SiNWs (32 µm thick)</td>
<td>−0.2 to +0.6 V</td>
<td>1 M KCl</td>
<td>1700</td>
<td>@ 50 mV/s</td>
<td>—</td>
<td>10¹</td>
</tr>
<tr>
<td>SiC NWs (6 µm thick)</td>
<td>−0.2 to +0.6 V</td>
<td>3.5 M KCl</td>
<td>240</td>
<td>@ 100 mV/s</td>
<td>—</td>
<td>9</td>
</tr>
</tbody>
</table>

**Devices**

<table>
<thead>
<tr>
<th>Electrode material</th>
<th>Electrochemical</th>
<th>Electrolyte</th>
<th>Capacitance per substrate area (µF cm⁻²)</th>
<th>Energy density (nWh cm⁻²)</th>
<th>Number of cycles</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Li-pre-treated SiNWs</td>
<td>0 to 2.5 V</td>
<td>NEt₄BF₄</td>
<td>45 × 10¹ to 90 × 10¹</td>
<td>@ 2.44 mA/cm²</td>
<td>—</td>
<td>5</td>
</tr>
<tr>
<td>P-SiNWs (11 µm thick 100 nm)</td>
<td>0 to 1.0 V</td>
<td>1 M NEt₄BF₄</td>
<td>7</td>
<td>@ 5 µA/cm²</td>
<td>2 × 10² (0.5% loss)</td>
<td>6</td>
</tr>
<tr>
<td>N-SiNWs (20 µm thick 50 nm)</td>
<td>0 to 1.0 V</td>
<td>1 M NEt₄BF₄</td>
<td>10</td>
<td>@ 10 µA/cm²</td>
<td>2.5 × 10⁵ (1.8% loss)</td>
<td>7</td>
</tr>
<tr>
<td>N-SiNWs (50 µm thick 20−200 nm)</td>
<td>0 to 1.2 V</td>
<td>1 M NEt₄BF₄</td>
<td>51</td>
<td>@ 10 µA/cm²</td>
<td>2 × 10⁵ (5.6% loss)</td>
<td>This study</td>
</tr>
<tr>
<td>Porous Si (43 µm thick)</td>
<td>0 to 0.5 V</td>
<td>0.25 M NEt₄BF₄</td>
<td>120</td>
<td>@ 10 mV/s</td>
<td>4.2</td>
<td>10</td>
</tr>
<tr>
<td>Porous Si (48 µm thick)</td>
<td>—</td>
<td>3.8 M H₂SO₄</td>
<td>2.9</td>
<td>—</td>
<td>—</td>
<td>11</td>
</tr>
<tr>
<td>Gold coated porous Si (43 µm thick)</td>
<td>—</td>
<td>3.8 M H₂SO₄</td>
<td>320</td>
<td>—</td>
<td>—</td>
<td>11</td>
</tr>
<tr>
<td>Gold coated porous Si (48 µm thick)</td>
<td>—</td>
<td>1 M LiClO₄ in PC:DMC (1:3)</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>11</td>
</tr>
</tbody>
</table>
silicon or SiC DLC in other papers.\textsuperscript{6,8} Such high double layer capacitance value is maintained when the BET surface area is increased with lithium insertion pre-treatment. The authors mentioned a SiNWs loading up to 1 mg cm\(^{-2}\) of a symmetrical device using N-SiNWs 50 µm length 20–200 nm \(\phi\); insert: detail of a charge discharge cycle of the same device @ 10 µA cm\(^{-2}\).

![Figure 3.](image-url) Long term cycling behavior in 1 M NEt4BF4 in PC @ 5 µA cm\(^{-2}\) of a symmetrical device using N-SiNWs 50 µm length 20–200 nm \(\phi\); insert: detail of a charge discharge cycle of the same device @ 10 µA cm\(^{-2}\).

4. Conclusion

Literature survey of silicon based electrodes for EDLC applications evidences that (i) highly n-doped silicon exhibits low EDLC capacitance value \((\approx 6 \mu F \cdot cm^{-2})\), (ii) the increase in capacitance can be achieved by increasing the surface using N-SiNWs structuration and it is directly linked to the surface enhancement factor and (iii) several strategies are efficient to grow SiNWs with significant surface capacitance \((440 \mu F \cdot cm^{-2})\) directly on doped silicon substrate which is interesting for assembling ECs microdevices. SiCNWs also present an interesting alternative to SiNWs due to their higher capacitance in mild aqueous electrolyte but this need to be confirmed in standard organic based electrolyte.

Symmetrical microdevices based on two identical silicon based electrodes can be operated in organic based electrolytes with 1.2 V voltage window. By tuning the electrode nanostructuration, the device’s capacitance can be enhanced up to 51 \(\mu F \cdot cm^{-2}\), thus retaining an energy density of 10 nWh cm\(^{-2}\) \((37 \mu J \cdot cm^{-2})\). The devices show excellent cycling efficiency over more than 2000 cycles. These values could be improved by increasing the surface enhancement factor. This is the topic of our current research which aims at growing silicon nanotrees with improved surface capacitance. Another way to improve the energy density is the use of ionic liquids which can help to further enlarge the operating electrochemical window. Finally, SiNWs microdevices show up to \(2 \times 10^7\) cycles which is quite promising for long term cycling efficiency that will have to be evidenced in the future on longer cycle life.

Acknowledgments

The authors thank the French DGA and CEA for financial support. French National Research agency and European Project FP7 are also greatly acknowledged for financial support with respectively the framework of ISICAP project and NEST Project.

References