A fully digital clock and data recovery with fast frequency offset acquisition technique for MIPI LLI applications

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Abstract: A new frequency offset compensation technique for the MIPI Low Latency Interface (LLI) application is proposed. The proposed clock and data recovery (CDR) circuit has a composite structure of bang-bang and oversampling phase detectors with an offset estimator. Digitally estimated frequency offset is used to determine the gain of the 2nd order digital CDR. An elastic FIFO for the oversampled multi-phase data stream is not needed, because the proposed offset estimator can compensate for frequency offset instead. With a frequency offset ranging from $-60,000$ ppm to $+60,000$ ppm, the proposed CDR has a very fast and almost constant lock acquisition time of less than 15 unit intervals and a short recovery logic latency of 1 unit interval. The proposed digital CDR is implemented using 65-nm CMOS technology. It consumes 5.1 mW from a 1.2-V power supply at 5.8 Gb/s.

Keywords: CDR, clock and data recovery, LLI, low latency interface, frequency offset, MIPI

Classification: Integrated circuits

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1 Introduction

The fast advance of interconnection technologies has reduced the cost of electronic components in mobile devices. In a conventional mobile device, a modem usually requires its own discrete DRAM in addition to DRAM attached to an application processor. However, with a low latency interface such as MIPI LLI (Low Latency Interface), the modem and application processor can share a memory, and phone manufacturers can remove the DRAM dedicated to the modem. The round-trip latency required to maintain enough read throughput for cache refill is shorter than 100 ns in MIPI LLI. Hence, the CDR for MIPI LLI has to extract clock and data with a low latency, and the lock acquisition time must be much faster than that of the conventional phase tracking CDR. Furthermore, these requirements for MIPI LLI must be met for a wide range of frequency offsets.

Some previous digital CDR architectures [1, 2, 3] have realized fast response recovery with a moderate frequency-offset tracking range, and another digital CDR architecture [4] has provided the advantage of an offset-free tracking ability. However, these designs have the disadvantage of a long lock-acquisition time due to slow accumulation of the integral path. An oversampling architecture [5] significantly reduced lock acquisition time using multi-phase blind oversampling. But the latency in the CDR was increased, compared with other CDR architectures [1, 2, 3, 4] due to a wide examining window for its threshold decision technique. This paper proposes a fully digital CDR with a fast frequency-offset acquisition technique. Instead of using an elastic FIFO, the proposed CDR employs an offset estimator to quickly calculate the frequency offset and compensate for it. So, the proposed CDR can realize fast lock acquisition and low logic latency for MIPI LLI applications.

2 Proposed CDR architecture

A conventional digital phase-tracking CDR and an oversampling CDR are shown in Figs. 1 (a) and (b), respectively. The accumulator of the conventional CDR with a bang-bang phase detector (BBPD), shown in Fig. 1 (a), usually spends microseconds integrating the static frequency errors. In contrast, the oversampling CDR in Fig. 1 (b) has a short lock-acquisition time due to blind oversampling. However, it has a long latency from its deep elastic FIFO. Oversampled input data bits are voted and then enter an elastic FIFO, which is used to adapt the frequency difference between two clock domains. Thus, an additional delay occurs due to the FIFO, and the logic complexity is also increased.

Fig. 2 shows the proposed digital CDR architecture, which employs a

Fig. 1. Block diagram of CDR: (a) Conventional digital phase tracking CDR. (b) Conventional digital oversampling CDR.

Fig. 2. Proposed digital CDR architecture.

composite structure of BBPD and oversampling phase detector (OSPD) with a frequency offset estimator. The proposed architecture employs tracked oversampling scheme to compensate the frequency offset using a multi-phase interpolator. Just like in a conventional digital phase-tracking CDR, shown in Fig. 1 (a), there is a proportional path from the BBPD and an integral path from the frequency offset estimator. Four-phase (0° , 90° , 180° , and 270°) input data are used for the OSPD to extract the current edge position signals. The two-phase input data (0° and 180°) are also used for the BBPD to operate the proportional path. The offset estimator estimates the magnitude and polarity of the frequency offset by monitoring the flow of the edge position signal from the OSPD. Then, the estimator first sets the proportional gain ($K1$) and forces the accumulator to have a proper value of $K2$ based on the estimated frequency offset. Therefore, the proposed CDR does not need a long sync pattern and an elastic FIFO, and it can quickly lock the recovery loop. In addition, using the edge position signals from the OSPD, the bit selector immediately selects the input data closest to the eye center among the oversampled multi-phase data, and it successfully recovers the data. The procedures of frequency offset compensation and data recovery are elaborated on in the next section, with more circuit details.

3 Proposed frequency acquisition method

Fig. 3 shows the proposed phase detector which is a composite of the BBPD and the OSPD. Because the BBPD requires 0° and 180° data, the 4x oversampling scheme for OSPD is adopted instead of a 3x or 5x oversampling scheme. An input bit has 4 phase boundaries, and two adjacent oversampled data are XORed and generate edge position signals

Fig. 3. Composite phase detector of BBPD and OSPD.

(A, B, C, D) which indicate whether an edge occurs at the phase boundary between two adjacent data. The BBPD is used for the proportional path to track the phase, and its output signals (X, Y) indicate only the polarity of the phase offset: whether the clock is leading (X is high) or lagging (Y is high) the data. Through this BBPD operation, the proposed CDR can induce a 0° phase clock at the center position of the data eye, and the output of the OSPD (C or D) is set to high. Fig. 4 shows a simplified flow chart of the offset estimator operation. The estimator monitors whether the outputs (A, B, C, D) from the OSPD are changed. If they are changed, the internal counter counts the bit intervals between the two successive events of the edge-position signal change. Because there are 4 phase boundaries, the output of the OSPD is changed when the phase shift reaches 0.25 UI. The absolute value of the frequency offset, therefore, can be calculated as shown below in Eq. (1):

$$|Frequency\ offset| = \frac{0.25UI}{N_{edge_interval}}. \quad (1)$$

where $N_{edge_intervals}$ represents the clock cycles counted by the internal counter. Depending on the calculated frequency offset, the estimator sets the proportional gain (K1) and the accumulation gain (K2) based on Table I. The polarity of the frequency offset is also set by the estimator based on the signal flow of the edge position signals. The example waveforms in Fig. 5 illustrate the operation of the frequency offset compensation. In step 1, the frequency offset is estimated. The edge-position signal is changed from B to A after 10 clock cycles, which indicates a 0.25-UI phase shift for 10 clock cycles, and the estimated frequency offset is

Fig. 4. Simplified flow chart for the offset estimator.

Table I. Lookup table for K1 and K2.

offset estimation [ppm]	K1 & K2	offset estimation [ppm]	K1 & K2
0 ~ +3750	0	+30000 ~ +33750	8
+3750 ~ +7500	1	+33750 ~ +37500	9
+7500 ~ +11250	2	+37500 ~ +41250	10
+11250 ~ +15000	3	+41250 ~ +45000	11
+15000 ~ +18750	4	+45000 ~ +48750	12
+18750 ~ +22500	5	+48750 ~ +52500	13
+22500 ~ +26250	6	+52500 ~ +56250	14
+26250 ~ +30000	7	+56250 ~ +60000	15

*If the frequency offset is less than zero, the polarities of K1 and K2 are inverted.

Fig. 5. Timing diagram of the frequency offset compensation.

25,000 ppm. Moving from B to A shows positive offset polarity, which means the clock on the transmitter side is faster than the clock on the receiver side. In step 2, the estimator sets both K1 and K2 to 6, in accordance with Table I, and the polarity to “01.” In step 3, The BBPD starts to operate in the proportional path with the programmed K1, and the estimator continuously monitors whether either C or D is high, which means the rising edge of the 0°-phase clock is located near the eye center. In step 4, if the 0°-phase clock is out of eye center, as in this example (C goes down, and B becomes high), the estimator increases the K1 by 1. The increased K1 enhances the tracking speed for the BBPD. In step 5, eventually the 0°-phase clock is dithered at the eye center so that C and D are toggled interchangeably. By adaptively compensating for the gain of the 2nd-order recovery loop, the proposed CDR can dramatically reduce the accumulation time and realize very fast lock acquisition in a wide range of frequency offsets.

4 Simulation results

The core circuit is fully implemented using a 65-nm CMOS process. The proposed digital CDR is tested with Tx, Rx, and clocking circuits implemented as analog behavioral models. A 2^7-1 PRBS pattern is used for post-layout simulation. Simulation results show that the proposed CDR consumes 5.1 mW from a 1.2-V power supply at 5.8 Gb/s. Fig. 6 (a) shows the lock acquisition time as a function of frequency offset for the conventional CDR and the proposed CDR. While the lock acquisition time of the conventional CDR increases exponentially as the frequency offset increases, the lock acquisition time of the proposed CDR remains less than 15 unit intervals with the frequency offset range of $\pm 60,000$ ppm. Fig. 6 (b) shows the phase error results when varying the frequency offset. In this simulation, RJ (random jitter) with normal Gaussian distribution is also applied. The peak-to-peak value and the standard deviation of the RJ are 0.1 UI and 0.018 UI, respectively. The phase errors of the proposed CDR are slightly reduced compared to that of the conventional CDR, even though the lock acquisition time is reduced significantly. Jitter tolerance is also simulated and compared with a sinusoidal jitter (SJ) mask of MIPI M-PHY which is widely used for MIPI LLI applications. As shown in Fig. 6(c), jitter tolerance of the proposed CDR meets MIPI M-PHY requirements, and the simulation results are well matched with the theoretical estimation. The applied SJ can be expressed as $A_j \sin(2\pi F_j n)$ [5], where A_j is the amplitude of the jitter, F_j is the normalized jitter frequency defined as the

Fig. 6. Post simulation results: (a) lock acquisition time vs. frequency offset. (b) phase error vs. frequency offset. (c) jitter tolerance.

ratio of sinusoidal jitter frequency to the baud rate, and n is the index of the data bits. The maximum phase change speed of the sinusoidal jitter is then $2\pi A_j F_j$ [UI/UI]. The test pattern of 2^7-1 PRBS data has a guaranteed transition density of $1/7$, and the maximum phase step of the proposed data recovery core is $2/64$ UI. So the low frequency jitter tolerance can be expressed as the following in Eq. (2).

$$JitterTol_{(low-freq)} = \frac{1}{224\pi \times F_j} [UI]. \quad (2)$$

On the other hand, the high frequency jitter tolerance for this logic is 0.5 UI because the BBPD is employed. As shown in Fig. 6 (c), the simulated jitter tolerance is well-matched to the theoretical estimation results. The simulated high-frequency jitter tolerance of 0.48 UI is quite close to the theoretical result of 0.5 UI. The simulated corner frequency is about 16.4 MHz, which is also close to the theoretical estimate of 17.1 MHz.

5 Conclusions

We demonstrated a fast frequency-offset acquisition technique for digital CDRs. The proposed phase detector and the frequency offset estimator can quickly adjust the 2nd order recovery loop based on a digitally estimated frequency offset. By adjusting the proportional gain and reducing the accumulation time, the proposed CDR realizes a lock acquisition time of shorter than 15 unit intervals with a frequency offset range of $\pm 60,000$ ppm. The bit selector utilizes the edge position information from the OSPD and almost immediately recovers input data, without an elastic FIFO operation. Furthermore, phase error and jitter tolerance are not degraded compared to the conventional CDR. The proposed CDR can be attractive to the digital CDR of MIPI LLI applications which require fast lock-acquisition and low latency.

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