A 6-bit 1 GS/s DAC using an area efficient switching scheme for gradient-error tolerance

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Abstract: This paper presents a 6-bit current-steering DAC fabricated in 65 nm digital CMOS process. In order to compensate for the systematic errors on the current sources, a novel switching scheme is proposed which can theoretically cancel out linear and quadratic gradient errors. Its implementation only requires reasonable number of current sources without increasing in the design complexity. The measured DNL and INL are 0.012 LSB and 0.023 LSB respectively. At the sampling rate of 1 GS/s, 5.9 bit ENOB and 51.4 dB SFDR at Nyquist frequency are achieved.

Keywords: DAC, switching scheme, gradient error

Classification: Integrated circuits

References


1 Introduction

Digital to Analog Converters (DACs) are widely adopted as critical interfaces in applications such as signal process, wireless communication and measurement systems. In such applications, DACs with high-speed, high-linearity
and low-cost are often required which makes current-steering architecture the best choice. Since the linearity of current-steering DAC mainly depends on the matching performance of current sources, this architecture is highly susceptible to process variation and surrounding environment. However, as the technology node continually shrinks to nanometer dimension, both inter-die and intra-die process variations become more significant [1]. The advanced technology also leads to improvement in SoC integration which further complicates the DACs’ implementation environment. Large-size devices can compensate for random errors derived from process fluctuation. And this, in turn, makes systematic gradient errors more prominent. Besides, the gradient error profile is unpredictable before measurement and suffers from lot-to-lot variability. A switching scheme can be used to reorganize the unary current source array and prevent the accumulation of non-linearity errors. In this paper, a 6-bit 1 GS/s current-steering DAC is presented which employs a gradient-error tolerant and area efficient switching scheme. Measurement shows that it achieves 0.012 LSB DNL and 0.023 LSB INL respectively.

The following part of the paper is organized as follows: In Section 2, the proposed switching scheme is introduced. The architecture and related design considerations of the DAC are briefly described in Section 3. The measurement results are given in Section 4. Finally, the conclusion is presented in Section 5.

2 Proposed switching scheme

Since the current source array takes a large area in the chip, it suffers from several kinds of systematic errors [2, 3]. There are linear gradient errors caused by oxide thickness and doping variation across the wafer or by the voltage drop along the power and ground lines. Meanwhile, there are quadratic gradient errors originated from temperature or die stress. Generally, the systematic errors of a single current source unit can be modeled by a superposition of both linear components and quadratic components which can be expressed by the following equation:

\[
\xi_{\text{unit}} = c_{\xi_{1}}x + c_{\xi_{2}}y + C_{1} + c_{\xi_{q_{1}}}x^2 + c_{\xi_{q_{2}}}y^2 + c_{\xi_{q_{3}}}xy + C_{2}.
\]

(1)

where \((x, y)\) is the coordinate of the unit. A unary weighted current source is often composed by multiple units. If these units are chosen arbitrarily from the current source array, the systematic errors may accumulate in some current sources which leads to linearity degradation. To prevent this, many switching scheme are developed to change the switching sequence of the current sources. A switching scheme is proposed in [4] which theoretically can cancel the linear and quadratic gradient errors at MSB level completely. The main idea is to split a unary current source in each row and in each column and then mirror the matrix to construct a new pattern as shown in Fig. 1. Due to the symmetry and uniformity of this scheme, the first-order and second-order gradient errors are canceled.
Fig. 1. Switching scheme for 6-bit MSB unary current sources (units of current source 0 are emphasized).

However, this scheme requires too many current sources to implement. For n-bit unary decoding, it needs $2 \cdot 2^n$ elements. In order to minimize the area and still maintain the switching scheme’s properties, a hierarchical unary decoding approach is employed. In the top hierarchy, construct a matrix to implement only $n/2$ bit unary decoding. Then replace each element in this matrix with a low level matrix which contains $2^{n/2}$ elements. With this strategy, a square array is obtained and only $2 \cdot 2^{3n/2}$ current sources are required. Specifically, to implement a 6-bit unary decoding, the 3-bit pattern in Fig. 1 is used as the top hierarchy. Then, each element in Fig. 1 is replaced by a $2 \times 4$ matrix. Thus, each unary current source contains 16 scattered units and only 1008 units in total are enough for the implementation.

For a unary current source with N units, the total error caused by gradient errors is:

$$\xi_{CS} = c_{l1} \sum_{i=1}^{N} x_i + c_{l2} \sum_{i=1}^{N} y_i + c_{q1} \sum_{i=1}^{N} x_i^2 + c_{q2} \sum_{i=1}^{N} y_i^2 + c_{q3} \sum_{i=1}^{N} x_i y_i + C. \quad (2)$$

To improve the linearity, all the errors should be equalized as much as possible. Because the top hierarchy matrix before mirrored has a “Sudoku-like” pattern, with exact one unit in each row and one unit in each column, the terms $\sum_{i=1}^{N} x_i$, $\sum_{i=1}^{N} y_i$, $\sum_{i=1}^{N} x_i^2$, $\sum_{i=1}^{N} y_i^2$ are the same for every current source. As the matrix mirrored along the y axis, there are two units of each current source located in symmetrical positions in each row with coordinate as $(x_i, y_i)$ and $(-x_i, y_i)$. Therefore, the term $\sum_{i=1}^{N} x_i y_i$ cancels each other in the same row and results in same sum for the top hierarchy matrix.

The next step is to replace each element in top hierarchy matrix by a low-level matrix. The term $\sum_{i=1}^{N} x_i y_i$ would still be nullified by the symmetrical pattern. However, for the linear terms and quadratic terms, extra measures should be taken to restore its error-averaging characteristic. As shown in Fig. 2, the low-level matrix is rotated in one direction and flipped in lower half part of the top hierarchy matrix. Units labeled with the same number take all the positions in the matrix one by one. Supposing the original coordinates of top hierarchy units locate at the center of each low-level matrix, in the $x$ dimension, half of the units are with coordinates $x_i + 1/4$ and the other half $x_i - 1/4$. On the other hand, in the $y$ dimension, the units are equally distributed in the positions with $y$-coordinates $y_i + 3/8$, $y_i + 1/8$, $y_i - 1/8$. 
and \( y_i - 3/8 \). Thus, the linear terms remain the same as before.

As for the quadratic terms, there is no way to make the elements distributed in each row and column with the limited number of current sources. However, this problem can be tackled by finding some position combinations which have the same quadratic error sum and put these unary current sources in these spots. From the observation of Fig. 3, if \( A + D = B + C \) is fulfilled, the following equation is always true:

\[
(A + d)^2 + B^2 + C^2 + (D + d)^2 = A^2 + (B + d)^2 + (C + d)^2 + D^2. \tag{3}
\]

This rule can be applied to higher order matrix. To simplify the analysis, redefine the coordinate system where every current source unit has an integer coordinates. Supposing 1 to 32 as the row numbers i.e. the \( y \) coordinates, fill them in a matrix as shown in Fig. 4, at least 4 combinations which have exactly the same quadratic sum can be obtained. If the unary current sources are placed in these positions, their quadratic gradient errors in the \( y \) dimension can be canceled out. With similar approach, the quadratic gradient errors in the \( x \) dimension can also be canceled out. Actually, these positions can be realized just by rotating the low-level matrix in the way shown in Fig. 2. To verify this scheme, a 6-bit current-steering DAC is mathemat-
Fig. 5. The linear (left) and quadratic (right) gradient error distribution used in the mathematical model.

Table I. Comparison of linearity errors introduced by gradient error with other switching schemes.

<table>
<thead>
<tr>
<th></th>
<th>[2]</th>
<th>[4]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>DNL (LSB)</td>
<td>0.12</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>INL (LSB)</td>
<td>0.33</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Number of Current Sources</td>
<td>1024</td>
<td>8192</td>
<td>1024</td>
</tr>
</tbody>
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ically modeled by ideal current sources (infinite output impedance and no random variation) with only gradient errors. The gradient errors are modeled by superposition of both linear and quadratic errors as shown in Fig. 5. This switching scheme and other methods including $Q^2$ random walk [2] and the scheme proposed in [4] are implemented on this model. The simulation results are summarized in Table I. No matter how the error pattern shifts and rotates, results show that the proposed scheme can guarantee all the unary current sources have the same current and less current sources are needed.

3 Circuit implementation

As shown in Fig. 6, a 6-bit current-steering DAC is designed based on the proposed switching scheme. A fully unary architecture is chosen which guarantees monotonicity and enables flexibility to perform switching scheme. It mainly consists of the current sources and current sources selection circuits. The 6-bit input digital codes are first converted to 63-bit thermometer codes by a simple row-column decoder. The thermometer codes are used as control signals to steer the current to drive the off-chip resistors. The fully differential output swing is 600 mV with a 1.2 V supply voltage.

With each current source split into 16 units, 1008 identical current generators are used to construct a regular array and the vacant positions are filled by a bias and 15 dummy units. A high-gain OpAmp is used as a voltage-to-current converter to provide a steady reference current. In order to enhance the output impedance, a cascode structure is selected to implement the unit. The devices are considerably enlarged to compensate for the random errors.
due to process variation. As each unary weighted current source takes an area of 1000 \( \mu m^2 \) in total, the estimated current value standard deviation is less than 0.1% for a 65 nm CMOS process [5], which leaves the systematic gradient error the main source of the non-linearity.

All the current sources are controlled by switches. The control signals of the switches are important for the dynamic performance. Latch is adopted to align the differential control signals to prevent glitches derived from their transmission delay differences. Following the latch, the cross point of control signals is shifted to higher position by de-glitch circuit which suppresses current source’s drain voltage variation. And then, to reduce signal feed-through, the swing of the control signals is reduced to 400 mV from rail-to-rail by Swing Reduce Drivers (SRD).

4 Measured results

The DAC is fabricated in 65 nm 1P8M CMOS process and the micrograph of the chip is shown in Fig. 7. The core blocks occupy an area of 870 \( \mu m \times 600 \mu m \). The current sources are laid out according to the switching scheme.
Fig. 8. Measured output spectrum for a 489 MHz output signal at 1 GS/s.

Fig. 9. Measured SFDR and SNR performances at 1 GS/s.

mentioned above with two extra rows and columns added to reduce edge effects. In addition, the array is surrounded by wide guarding rings and placed far from the decoder to block the noise from the digital circuits. To ease the measurement, a parallel to serial converter is integrated in the chip which reduces the requirement for input data rate. An 80-pin CQFP is chosen as the chip’s package. The experimental results show that the DAC consumes 35 mW power from a 1.2 V supply voltage. With a 1 GSample/s data rate, the DAC achieves 37.52 dB SNR and 51.4 dB SFDR for a 489 MHz output signal as shown in Fig. 8. The measured SFDR and SNR performances are shown in Fig. 9 as function of signal frequency at 1 GS/s.

To get a rough idea of the influence of process variation, the 15 dummy current source units are measured. The error profile is shown in Fig. 10, its obvious that the current sources are not ideally matched with each other. The edge effect influence is evident and an approximate linear gradient error can be seen that may be derived from voltage drop along the ground line or doping gradients. The static performances are depicted in Fig. 11 and Fig. 12 in which INL and DNL are 0.023 LSB and 0.012 LSB respectively. The INL performance can be normalized to 0.368 LSB, i.e. 10-bit static linearity is achieved. The 2nd order gradient error shown in the INL is mainly caused by the current source output impedance variation during operation. The high linearity proves that the proposed switching scheme can reduce the
systematic gradient errors effectively.

5 Conclusion

A novel switching scheme is proposed in this paper. The method can theoretically cancel out both the linear and quadratic systematic gradient errors for unary weighted matching elements. This property is important for applications where high-precision matching is required or the error profile is unpredictable. A 6-bit 1 GS/s current steering DAC using this switching scheme is designed and fabricated in 65 nm CMOS process. The DAC achieves high linearity with reasonable number of current sources.
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