Femtojoule/bit integrated nanophotonics based on photonic crystals

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Abstract: This review article shows that the photonic-crystal nanocavity technology has enabled various nanophotonic devices, including all-optical switches, all-optical memories, electro-optic modulators, and lasers, which can operate with extremely-small consumption energy, owing to their very tight light confinement. These wavelength-scale largely-integrable low-power photonic devices are promising for realizing a dense photonic network in a processor chip, which will enable high-performance information processing with small consumption power and reduced heat generation.

Keywords: photonic crystal, photonic integrated circuit, photonic network on-chip, optical interconnect, optical RAM

Classification: Fiber optics, Microwave photonics, Optical interconnection, Photonic signal processing, Photonic integration and systems

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1 Introduction

1.1 Confronting issues for future ICT

Considering recent remarkable exponential growth of Internet, it is now apparent that the consumption energy of information and communication technology (ICT) will soon be a serious issue for our global economy and environment [1, 2]. If we classify ICT with its length scale, the long-distance communication is now dominated by photonics and the short-distance one is still mostly managed by electronics. In ICT, the most of energy is consumed at its rather short distance part with electric systems, such as network routers and data centers. More specifically, the energy is consumed in high-bit rate processor chips in those electric systems and their accompanying cooling systems. Hence, we have to reduce the energy consumption and heat generation in these chips to solve the aforementioned issue.

The energy consumption and heat generation in chips have recently become an urgent matter for chip makers, and there are a number of researches to solve this problem currently undergoing. If we look inside chips, more and more energy is now consumed not in transistors but in electric wirings. It was reported that more than half energy is consumed in wiring [3]. The wiring is now consisting of a large number of metal layers with spaghetti-like labyrinth. In addition, recent chip designs rely on the many-core architecture as shown in Fig. 1 (a). For instance, the latest one employs a network-on-chip (NoC) design [4] with 80 cores in which complex inter-core communications are handled by on-core micro-routers and 28% of the energy was consumed by these routers [5]. It indicates that the most critical issue will be how to manage networking in a small world efficiently.

1.2 Why do we need a photonic network in a chip?

In terms of signal transportation and communications, it has been said that photonics is generally better than electronics. This has been proven at long distance when copper cables were replaced by optical fibers. This transition

Fig. 1. History of processor chip evolution (a) and future of photonic network chips.

has started from long-haul backbones and is now intruded down to fiber-to-the-home (FTTH). This is a natural consequence from the fact that copper cables suffer from ohmic and radiation loss when the frequency goes up, though optical fibers do not. Generally, as the communication bandwidth increases, photonics would outperforms electronics at a much shorter length scale. Optical interconnect has been already introduced in rack-to-rack connections (even board-to-board) in high-performance computers consisting of a large number of processors.

In fact, if it comes to communications in “chips”, electric communications are facing other problems. First, electric wirings require more volume in order to reduce the RC delay at a higher bit rate, though the available volume is limited in a chip. Second, they inevitably consume a certain amount of energy for charging wires. This charging energy is restricted by the residual capacitance of wirings and the driving voltage of transistors, and is estimated to be larger than several fJ/bit [6]. As the bit rate goes up, it becomes more difficult to reduce these two factors, though there are no such issues in photonic wirings. One of the most critical issues is the energy cost per a single bit operation. It was predicted that if the performance of the processor chips will progress in the same rate as today, we should continuously reduce the energy cost per bit in a chip. Although currently hundreds of fJ/bit is allowable, we should achieve an order of fJ/bit in 2025 [6]. Note that this value is already smaller than the charging energy for wires.

In addition, some of photonics components and functions, such as photonic switching, add/drop routing, and wavelength-division multiplexing (WDM), are known to be very effective for managing high-bit-rate network traffics. They should be also effective in a chip when the bit rate goes up, though they have been so far employed only in conventional networks (such as metro or backbone).

From these backgrounds, numerous efforts toward replacing copper wirings among chips or cores with optical links (chip-scale optical interconnect) has already begun. However, if we think of further evolved chips in future, it will be advantageous to introduce more sophisticated photonic network technologies into a chip, rather than simple point-to-point links. Such photonic network-on-chip design has already been proposed and studied in which one exploits the full advantage of various photonic networking functions [7, 8]. Probably, we will start with WDM matrix networks equipped with switches as shown in Fig. 1 (b). Then, we will add more advanced networking functions including more sophisticated switches, digital data recoveries, digital amplifiers, variable delays, and routers. This scenario predicts that we need to integrate a very large number of photonic devices in a single chip. For example, if we introduce 100 channel WDM networks in 100×100 cores (core size $0.1 \times 0.1 \text{ mm}^2$), the total number of photonic devices would be 10 million or more per chip. The integration density will be $10^5/\text{mm}^2$, and this means that the device footprint should be around or less than several μm , which is orders of magnitude smaller than that for conventional photonic devices.

Then, a question may arise: “How come is such large scale integration possible in photonics?” The photonic integration is still very much poorer than the electronic counterpart in spite of a long history of research efforts. However, if we look at Fig. 2, we can foresee some trend. Figure 2 shows a chronological record of number of transistors in a chip (known as Moore’s law) and a similar record for photonic devices in a chip. It is apparent that the photonic integration had started to rise up at around the turn of century. More important is that the rate of the increase is close to that of Moore’s law. If we simple-mindedly believe this trend, it predicts that we may be able to a million photonic devices in a chip around 2025.

Fig. 2. Moore’s law in photonics. Chronological record of the number of transistors and photonic devices in a chip.

However, this is a too optimistic view. The current increase in Fig. 2 is achieved by integrating conventional photonic devices, which will soon arrive at the limit due to their large footprint. As I mentioned earlier, a footprint of $10\mu\text{m}^2$ or less will be desired in future. Without introducing some form of *nanophotonics* technologies [9, 10], it will be impossible to continue the photonic Moore's law for the next decade. It is worth noting that Moore's law has been maintained by introducing a number of breakthrough technologies in electronics.

1.3 What can photonic crystal do?

The previous section clarified that we will need a certain technology satisfying the following points. (1) Footprint of $10\mu\text{m}^2$ or less. (2) Energy consumption of fJ/bit. (3) Large-scale integrability. (4) Low loss. (5) Capability of high-bit-rate network management. There would be several candidates for this goal: Si photonics, high-index-contrast waveguides, whispering gallery cavities, photonic crystals, and plasmonics. In this review paper, we intend to convince readers that photonic crystals will be most promising to satisfy these constraints.

Photonic crystals are artificial structures having a periodic modulation of the refractive index. Light waves in photonic crystals behave very similar to electrons in conventional crystals (having a periodic atomic lattice) [11, 12]. Consequently, the dispersion of light waves is highly modified from the original dispersion of composing materials, and exhibits a so-called photonic band structure. This leads to several remarkable characteristics, including slow light and negative refraction which arise from strong modification of frequency and spatial dispersions. One of the most important features is the appearance of a photonic band gap (PBG). Analogous to electronic band gaps which lead an electric insulator, the PBG leads to a photonic insulator which does not exist in nature. By employing photonic crystals having PBGs, we can realize ultrastrong light confinement with substantially low loss.

In fact, the reason why large-scale photonic integration has been so difficult can largely be attributed to a physical fact that "light is so difficult to confine in a small space". The photonic crystals with PBG can overcome this limitation, and various types of ultrahigh- Q wavelength-sized cavities have been realized in photonic crystals [12, 13]. Figure 3 shows some of those examples. It is worthwhile to note that wavelength-size cavities with Q higher than 10^5 can be realized only by photonic crystals at optical frequencies. These ultrahigh- Q nanocavities lead to the following three advantages. First, since most of photonic micro-devices are based on resonators, the smallness of cavities directly means a small device footprint. Second, large Q/V (V : the effective mode volume of a cavity) leads to large light-matter interactions (for example, large photonic local density of states) [8]. Third, ultrahigh- Q can realize a low coupling loss when coupled with input/output waveguides. Since these advantages are general, we can expect to realize various types of wavelength-sized photonic devices with substantially small consumption energy and low optical loss.

Fig. 3. Various high- Q designs for photonic crystal cavities. Q : cavity quality factor. V : effective mode volume of a cavity. λ : resonant wavelength, n ; refractive index. Details are described in Ref. [12].

This is the main reason why we chose photonic crystals for the target described in 1.2. In reality, however, there are many issues we should solve and develop for the target. Next, we describe some of technologies we developed.

2 Key technologies of photonic crystals

2.1 Modulated mode-gap cavities

Among various cavities in photonic crystals, we are especially interested in a particular class of cavities shown in Fig. 4. They are all consisting of a line defect in a photonic crystal with a certain spatial modulation. This line defect is a so-called W1 waveguide which is a single-mode radiation-free waveguide located within the PBG [12]. An important property of this W1 waveguide is that it has a mode gap below the cut-off frequency. Hence, when introducing a certain structural modulation, light confinement is achieved by a spatial modulation of the cut-off [12]. The resultant optical field mode is illustrated in Fig. 4(a) when colored holes are shifted toward outside by 3, 6, and 9 nm, respectively, which shows a formation of a nanocavity [14]. Readers may think that this is nothing different from simply terminating a waveguide to form a cavity, but such termination will heavily distort the field profile, thereby producing a large amount of radiation loss. That is, high Q cannot be achieved by simple termination. However, the field profile of width-modulated cavities mostly resembles that for the loss-free straight W1 waveguide since the introduced spatial modulation is so small. That is why it leads to ultrahigh- Q . The theoretical Q can be > 1 billion, and experimental $Q > 1$ million has been achieved for this type of cavities.

Similar confinement can be achieved by other types of spatial modulation,

Fig. 4. Modulated mode-gap cavities in photonic crystals. (a, b) Width modulated cavities. (c) Index modulated cavity. (d) Dynamic modulation by optical nonlinear process. (e) High- Q nanocavity formation by a scanning nanoprobes lithography.

such as locally varying the lattice constant [15] or the hole radius [16]. In addition, ultrahigh- Q nanocavities can be formed simply by modulating the refractive index for a homogenous line defect waveguide (Fig. 4(c)). We have demonstrated that a substantially small index modulation (less than 10^{-3}) is sufficient for making a wavelength-sized ultrahigh- Q nanocavity [17]. By using this feature, recently, we have successfully formed an ultrahigh- Q nanocavity on a straight line-defect waveguide by local oxidation of Si surface using scanning probe lithography technique (also known as atomic force microscopy lithography) (Fig. 4(e)) [18].

This feature can be also utilized for dynamic control of light confinement. Since modulated mode-gap cavities require very small modulation, we can control the confinement strength by a slight change of modulation, for example, via optical nonlinearity. We have demonstrated that a light pulse stored in an ultrahigh- Q cavity can be dynamically released by applying another optical pulse causing nonlinear modulation of light confinement (Fig. 4(d)) [19].

2.2 Buried-heterostructure-induced cavities

When one applies a nanocavity for devices based on a certain light-matter interaction, it would be better to embed an active material only within a cavity. We can realize such an arrangement by employing the modulated

Fig. 5. (a, b) Buried-heterostructure cavity. (c) InGaAs quantum wires embedded in InGaAsP layers. (d) InGaAsP/InP buried heterostructure cavity in an InP photonic crystal.

mode-gap cavity design in 2.1. If we embed an InGaAsP region in an InP photonic crystal line defect, the InGaAsP region acts as a sufficient index modulation to form a high- Q nanocavity as shown in Fig. 5 (a, b). Hereafter, we call this cavity a buried heterostructure (BH) cavity.

In principle, this structure can be fabricated a combination of etching and regrowth. In this design, however, the flatness of the top slab surface is crucial to achieve a high Q because a 10-nm bump will drastically reduce Q . It may seem that it would be rather difficult to make high Q cavities by etching and regrowth, but it is indeed possible to obtain a flat surface after overgrowth by sophisticated etching-and-regrowth techniques. Figure 5 (c) shows an old example of etching- and-regrowth for nanostructures, where 40-nm-wire-InGaAs quantum wires were embedded in InGaAsP layers by metal-organic vapor-phase-epitaxy overgrowth [20]. Quantum wires fabricated by etching were successfully embedded in InP and InGaAsP, and the top surface of InGaAsP was perfectly flat, realized by mass transport of InP during the growth. (InP tends to exhibit a flat surface which has a minimum surface energy). In 2010, we have successfully fabricated the BH cavity design for lasers in photonic crystals (Fig. 5 (a)) by the etching-and-regrowth technique as shown in Fig. 5 (d) [21]. Here, an InGaAsP region is embedded in a line defect of InP photonic crystals, and the top InP surface is sufficiently flat. We will show later that this BH cavity can boost the performance of various devices.

2.3 Lateral p-i-n junction

In order to put photonics into a chip, it is crucial to realize fast and energy-efficient E-O/O-E conversions (lasers, detectors, and modulators). For this purpose, it is important to combine an ultrasmall p-i-n junction and a nano-

Fig. 6. (a) Si photonic crystal nanocavity with a lateral p-i-n junction. (b) Measured transmission spectrum showing ultrahigh- Q after the junction formation.

cavity. We have realized a Si photonic-crystal mode-gap modulated nanocavity equipped with a lateral p-i-n junction shown in Fig. 6(a) [22]. The p-i-n junction was formed by the ion implantation technique. For this configuration, it had been worried that the additional optical absorption in doped region would degrade cavity Q , especially for nanocavities for which the p-i-n junction should be located very close to the cavity core. However, we have demonstrated that if we appropriately choose the geometrical parameters, the device can maintain ultrahigh Q even after the junction formation [22], as shown in Fig. 6(b). By employing this tiny p-i-n junction, one can efficiently inject/extract carriers into/out of a sub-micron-scale core of a nanocavity. An important feature is that we can realize ultrasmall capacitance in this device configuration. A simple geometrical analysis shows that the structure in Fig. 6(a) would have a capacitance of tens of aF. Such ultrasmall capacitance would be very important to realize fast and energy-efficient photo-detectors and electro-optic modulators. We will show later actual device applications based on nanocavities with p-i-n junctions in 3.3 and 3.4.

2.4 Large-scale integrability

Another important issue is integrability. Concerning this issue, we have demonstrated a large-scale array of ultrahigh- Q coupled nanocavities shown in Fig. 7. The number of cavities integrated was 400 at largest. Each cavity was identical (in design) and we confirmed that the coupled array exhibited coherently coupled travelling modes [23]. This proved that large-scale integration is possible for photonic crystal nanocavities and we are now able to realize and control inter-cavity coupling in such a large-scale array.

Fig. 7. Large-scale array of ultrahigh-Q nanocavities in a Si photonic crystal. The largest $N = 400$.

3 Ultralow-power nanophotonics devices

As we wrote before, a large Q/V ratio should, in principle, lead to substantial reduction in consumption power for various photonic devices. In this section, we will show our recent studies of device applications, especially focusing on the consumption energy, by applying various technologies described in section 2. It will be understood that the above Q/V argument is too simple, and it is essentially important to employ appropriate structures, materials, and functions to fully extract the potential of photonic crystal nanocavities.

3.1 All-optical switches

One can realize an all-optical switch by introducing an optical nonlinear material in a resonator. The transmitted light intensity of the signal can be modulated by applying another optical control pulse which induces a shift of the cavity resonance via optical nonlinearity. For such switches, the switching energy is known to be proportional to V/Q [8]. However, a large Q also limits the operation speed. Therefore, it is crucial to combine effective optical nonlinearity with a nanocavity having Q appropriate for the operation speed.

With these constraints in mind, we fabricated all-optical switches as shown in Fig. 8(a) [24]. Although Kerr nonlinearity has been commonly employed for fast all-optical switches, we adopted carrier-based optical nonlinearity and chose quaternary compound semiconductor InGaAsP (PL wavelength is 1450 nm) which exhibits very large carrier-based nonlinearity at 1550 nm (via a combination of the band filling effect and carrier plasma dispersion). It has been known that the carrier-based effect can be much larger than the Kerr effect, but the former is slow because of the long relaxation time of photo-excited carriers in high-quality semiconductors (~ 10 ns). However, we found that the relaxation time is extremely short (~ 10 ps) for carriers excited in a nanocavity because photo-excited carriers rapidly escape out via fast diffusion process. Since the diffusion becomes faster for smaller cavities, we chose a so-called H0 cavity (shown in Fig. 8(a)) which is the smallest dielectric-core cavity ($V = 0.02 \mu\text{m}^3$) with $Q > 10^3$. Note that the smallness has two contributions. First, small V leads to large Q/V ratio with appropriate Q . Second, it leads to fast operation speed. Our calculation shows that the carrier escape time is 3.5 ps in H0 cavities which is much faster than

Fig. 8. All-optical switches by nanocavities. (a) Device and cavity structures, and the operation mechanism. (b) Experimental result of all-optical switching. The time-dependent output intensity from the device. (c) Comparison of various all-optical switches in terms of the switching energy and switching speed.

other types of photonic crystal nanocavities.

As a result, we have observed clear switching operation at room temperature as shown in Fig. 8(b). The switching time is 20–35 ps, and the switching energy is 420 aJ for 3 dB contrast; 660 aJ for 10 dB contrast. As far as we know, this is the smallest all-optical switching energy at room temperature. Figure 8(c) summarizes a comparison among various all-optical switches. Note that for conventional switches, the product of the switching energy and the switching time is almost constant. However, our switch is more than two orders of magnitude smaller in terms of this product, indicating our device has overcome the tradeoff. The reason is simply attributed to the smallness of our device. In electronic devices, such as transistors, it has been well established that as the footprint becomes smaller, the device operates faster with less consumption energy. However, this trend has not been so clear in photonics, mainly because as the device became smaller, the efficiency became worse due to poor light confinement. By employing photonic crystal nanocavities, it is now clear that the similar trend can be expected even in photonic devices. This should be indeed a good news for

photonic integration.

3.2 All-optical memories and RAMs

Next, we examine all-optical memories, especially random access memories (RAMs). This function is needed for various network management. For example, routers need high-speed memories to manage and synchronize the output timing of data packets. However, a RAM has been considered as one of the most difficult components for photonics. This is because optical RAMs generally need large power ($\sim$ mW) input to sustain stored information and the footprint is rather large ($\sim$ mm). Hence, it was difficult to seriously consider large-scale integration, though meaningful RAMs require a certain level of integration.

It has been well known that all-optical switches based on nonlinear resonators exhibits optical bistability at a certain condition. If we use these bistable states as bit information, these bistable switches function as all-optical bit memories in a similar way to a bistable memory based on a transistor. Although such nonlinear bistable switches require large input power, we can expect substantial reduction if we apply nanocavities. In 2005, we applied Si photonic crystal nanocavities to realize all-optical memories [25], and later achieved the operation power of $10\ \mu\text{W}$ by InGaAsP nanocavities [26]. However, this power is still too high for large-scale integration. In addition, the longest memory holding time was limited below 300 ns because the bistable state was broken by heating effect.

In fact, this shows that the device design for switches does not work well for memories. One reason is that the faster carrier escape means larger input power required to sustain the stored information. The second reason is that the heat management is more crucial for memories which need bias input. In order to solve these problems, we introduced a BH structure shown in Fig. 9(a, b). By employing the BH cavity design, it is now possible to strongly confine carriers and photons in the same space, thereby reducing the operation power. In addition, this design enables heat to escape very efficiently out of the cavity since InP has 17 times higher heat conductivity than InGaAsP.

Figure 9(c) shows a bit memory operation achieved in our device [27]. The device is driven by a bias optical power to keep the device at the bistable condition. At first, the output intensity is at the OFF state. When we inject a writing pulse, the output is switched to the ON state. Since this ON state is one of bistable states, it can be sustained even after the writing pulse diminishes. That is, the information is stored. Then, we read out the information by injecting a reading pulse. Finally, the stored information is erased by shutting down the bias power. Most importantly, the minimum bias power required for this operation is as small as 30 nW, which is more than 300 times smaller than the previous photonic crystal devices (and approximately $1/10^5$ of the power for conventional optical memories). In addition, we confirmed that the memory holding time is longer than 10 seconds, and there is no indication of heating. Consequently, the novel BH design has solved two

Fig. 9. All-optical memory by nanocavities. (a) Device structure. (b) Scanning electron microscope image. (c) Bit memory operation.

problems (poor carrier confinement and heating).

The achieved operation power and device footprint suggest that it would be possible to realize a 1 Mbit RAM with the consumption power of 30 mW and the footprint of order of mm. Since it was predicted that a certain type of future photonic routers need memories with the capacity of only ~kByte, we believe that there will be various applications for our optical RAMs.

To demonstrate RAM operation for high-bit-rate information, we integrated four-bit memories in a single chip, and performed a RAM subsystem demonstration with an all-optical serial-to-parallel converter [28] as shown in Fig. 10. A four-bit 40 Gbps signal was first converted to a four channel parallel signal by the converter, and then stored in nanocavity memories. Finally, the stored information was read out. This is the first demonstration of one-chip all-optical multi-bit RAM as far as we know.

3.3 Electro-optic modulators/Photo-detectors

As we showed in Fig. 6, we have realized ultrahigh- Q nanocavities with ultra-small p-i-n junction in Si photonic crystals. This structure is very promising for realizing efficient E-O/O-E conversion, which will be one of key components in photonic network on chip applications in Fig. 1. Since we can electrically inject carriers via the junction into the center insulating region where the cavity is located, we can expect electrically-driven switching operation in a similar way to all-optical switches in 3.1, which is merely an electro-optic (EO) modulator. We have demonstrated EO modulator operation with sufficiently low power ($2.1 \mu\text{W}$) as shown in Fig. 11 (a, b) [22]. The extinction contrast is 14.5 dB at 1.5 V. Furthermore, we have demonstrated a unique photo-detector employing the same Si nanocavity with p-i-n junction.

Fig. 10. 40-Gbps 4-bit all-optical RAM chip operation. Two types of four bit informations are stored and read out.

Fig. 11. (a) Transmission spectra at different applying voltages for Si photonic crystal nanocavity with p-i-n junction. (b) EO modulation. (c) Photo-current spectra for two-photon absorption in Si nanocavity with p-i-n junction. (d) Photo-current versus the input power.

Although Si is transparent at 1550 nm, this device can operate as an efficient photo-detector via two-photon absorption which is largely enhanced by four orders of magnitude owing to its large Q/V ratio. Figure 11 (c, d) shows this device performance, and it shows a surprisingly high quantum efficiency of 10% with extremely small dark current of 15 pA [29]. As was noted before, the electric capacitance of this structure is extremely small, which will be promising for power-efficient and ultrafast EO/OE conversions although the present data is still primitive.

3.4 Lasers

Another important EO converting device is a laser diode. Although there have been many trials to employ photonic crystal nanocavities for laser application, the performance had been limited because of the poor confinement of injected carriers and the insufficient heat management. We applied the BH cavity design in 2.2 to a photo-pumping laser as shown in Fig. 12 (a) to solve these two problems [21]. An InGaAsP active region is embedded in an InP photonic crystal nanocavity, which enables to strongly confine photons and carriers but escape heat effectively. As a result, we achieved room-temperature continuous-wave lasing with the record-low threshold power of $1.5 \mu\text{W}$, and 20-Gbps signal modulation with an energy cost of 8.8 fJ/bit which is over an order of magnitude smaller than that for conventional

Fig. 12. (a) Schematic of a photonic crystal nanocavity laser with an embedded active region. (b) Result of optically-pumped lasing oscillation. (c) Schematics of an electrically-pumped laser by a photonic crystal nanocavity with a p-i-n junction.

lasers. Recently, we combined the BH design and the lateral p-i-n junction to form an electrically-driven laser as shown in Fig. 12 (c), and achieved room-temperature continuous-wave lasing for the first time for nanocavity-based lasers [30].

4 Conclusion

We hope to have convinced readers that the photonic-crystal nanocavity technology are now enabling a number of largely-integrable nanophotonic devices with a footprint of μm order and a consumption energy of an order of fJ/bit. The propagation loss of photonic crystal waveguides and photonic wire waveguides is a few dB/cm, which is small enough considering the probable device size. Owing to intrinsic high- Q designs, the coupling loss can be very small. Hence, we believe that photonic crystals can potentially satisfy the most of requirements for applications to large-scale photonic network on chip we showed in 1.2., although there will be obviously a number of hurdles to overcome for practical usage. An important next step is to demonstrate on-chip integration. We are currently working on this direction to demonstrate a large-scale integration of nano-devices and also integration of different functionalities in a single chip. Finally, we would like to emphasize that this integrated nanophotonics technology to implement a dense photonic network into a tiny chip would not be only for processor chips in computers, but it would be applied for any areas where a large amount of high-speed data should be processed with a consumption energy as small as possible.

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