A 3–5 GHz IR-UWB CMOS RF transceiver with RF notch filter

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Abstract: A fully integrated 3 ~ 5 GHz CMOS RF transceiver for IR-UWB applications is implemented in 0.18 μm CMOS technology. The integrated RF notch filter is employed to reject the nearby WiFi and WCDMA interferers. The low power digital impulse generator is used as the UWB RF transmitter. The measured sensitivity of the receiver is -65 dBm at 4 GHz with 1 Mbps PRF. And the measured energy efficiency per pulse is 20.6 pJ/bit. The current consumption of the receiver and transmitter including DA is 27.5 mA and 25.5 mA, respectively, at 1.8 V supply.

Keywords: UWB RF transceiver, digital impulse generator, RF notch filter

Classification: Integrated circuits

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1 Introduction

Since the Federal Communication Commission (FCC) released the

unlicensed Ultra-Wide Band (UWB) spectrum ranging from 3.1 GHz to 10.6 GHz, the Impulse Radio Ultra-Wide Band (IR-UWB) technology has attracted much attention as a solution of the location based systems (LBS), radar sensor, and WBAN (Wireless Body Area Network), as well as the WPAN data communication applications. As the strong candidate of IR-UWB applications, the low power WPAN and Location Based System have been considered in industry due to its low complexity, low power, and expected accurate resolution of the distance detection. In this paper, a non-coherent IR-UWB transceiver with the tunable transmitter is implemented on 0.18 μm CMOS process. Since the carrierless non-coherent UWB receiver has its wideband characteristics, in the actual channel the undesired out-band interferers is also received and mixed, which in turn degrades the receiver sensitivity seriously. However, although many recent literatures report the UWB RF transceivers [1, 2, 3, 4, 5], only few reports address how the rejection of such interferers would be filtered and rejected. To our field experience, the undesired signals such as 2.4 GHz ISM band and WCDMA are most harmful noise for the 3 ~ 5 GHz UWB RF. Up to now, the several previous reports describe the integrated RF notch filter or its performance along with the interference [3, 4, 5]. However, the system performance improvement such as BER and the sensitivity including the interferer condition have not been scrutinized deeply in these literatures. Therefore, in this work, the tunable active RF notch filter to mitigate the undesired jamming signal below 2.4 GHz is integrated in the RF front end side, and also the sensitivity improvement with the RF notch filter is presented comparing with the performance of the RF notch 'off' state. As for RF transmitter, the tunable transmitter is shortly introduced.

2 UWB RF transceiver circuit design

Fig. 1 is the overall block diagram of UWB RF transceiver. The RF front end of receiver contains LNA, S2D (single to differential) amplifier, RF notch filter, RF VGA, and envelope detector (multiplier). The first stage LNA is the conventional inductively source degenerated LNA with resistive shunt feedback for the wideband matching. As shown in Fig. 2, the S2D amplifier employs the common gate (CG) and common source (CS)

Fig. 1. Block diagram of full UWB RF transceiver.

Fig. 2. Single to differential (S2D) amplifier using cross coupled cascode combined with the shunt peaking load.

amplifiers. For the gain and phase balance between CG and CS stages, C_{add} is attached compensating the effect of C_{db7} , which is added to C_{gs1} in parallel. And also to enhance the bandwidth and gain over the UWB high frequency, the cross coupled cascode topology combined with the shunt peaking load is employed.

The tunable RF notch filter is integrated in the 3rd stage amplifier to mitigate the interferers below 2.4 GHz and its circuit topology is shown in Fig. 3. The resonance frequency of LC resonator in notch filter is trimmable with the digitally switched capacitor array. The cross coupled pair provides the negative resistance to cancel the equivalent resistance of LC resonator. By optimizing the control code of capacitor array and bias current of the cross coupled pair, the notch frequency trimming and the resonator Q enhancement are achieved independently.

Fig. 3. 3rd stage cascode amplifier with tunable RF notch filter.

The simulated gain and NF of the receiver RF front end with RF notch filter 'on'/'off' are presented in Fig. 4. The simulated gain is slightly above 40 dB over 3~5 GHz UWB band. The hollowed circles represent the gain and NF with RF notch filter 'on', and the solid lines with RF notch filter

Fig. 4. Simulated gain and NF of RF front end with RF notch filter 'on'/'off'.

'off', respectively. As shown in Fig. 4, the simulated rejection at 2.4 GHz with the RF notch filter is 15 dB. The notch frequency can be trimmed from 2.1 GHz to 2.6 GHz as well as the rejection level. The simulated NF is above 3.8 dB and nearly same for both cases.

As depicted in Fig. 5, the multiplier adopts the self mixing Gilbert cell mixer and the output load is an active load parallel with R1 and C1, which is a low pass filter. Hence the envelope signal of UWB impulse is detected and the RF carrier is filtered out. The detected envelope signal is amplified one more time at the final stage and RF carrier is filtered out by low pass filter composed of Rout and Cout. Since the multiplier determines the minimum detectable pulse amplitude, the receiver's sensitivity dominantly depends on the multiplier as well as LNA stages. The simulated minimum detectable envelope voltage at the input is 20 mVpp or less, which corresponds to -70 dBm at LNA input assuming that the RF front end gain is 40 dB.

Fig. 5. Circuit schematic of self-mixing multiplier.

The next stage VGA is designed to obtain the sufficiently high and variable gain for the desired receiver's dynamic range. The designed RF VGA is conventional differential amplifier with the tunable gate bias

voltage for the linear gain control [6]. The integrator is a simple active RC integrator with the single stage OTA. With the help of integrator, the abrupt noise and interference can be smoothed down and eliminated while passing by comparator. The final comparator consists of the differential amplifier (or limiter) and buffering inverter amplifier. The envelope signal is applied to the positive input port and compared with the digitally controlled reference threshold voltage biased at the negative input. Moreover, because the overall gain of comparator is very high, the output signal comes out like a digital pulse with some duration time, whenever the amplitude of input pulse signal is high enough to invoke the comparator circuit. The duration time of output digital pulse can also be tuned by threshold voltage control. The amplitude of output digital pulse signal rises up to 1.8 V through output buffer to drive the digital BB part.

The Fig. 6 illustrates the block diagram of the proposed CMOS fully digital pulse generator. The proposed pulse generator is composed of the unit pulse generator, the unit pulse combiner and envelope shaper, and the output buffer. The unit pulse generator is composed of the unit time (τ) delay cells and EX-OR based differentiator. The unit time delay cell depicted in Fig. 6 is the current starved type inverter. The delay cell is an essential block, because the carrier frequency of the UWB pulse is $1/2\tau$. By controlling the inverter current, the delay time can be trimmed. And the number of the combined unit pulses determines the UWB pulse duration, in other words, the signal bandwidth. For example, when τ is 125 ps and the 8 combined pulses are used, the center frequency is 4 GHz ($1/(2 \times 125 \text{ ps})$) and pulse duration is 2 ns ($250 \text{ ps} \times 8$), which corresponds to 500 MHz bandwidth. As well as the variable unit time delay, the number of the combined pulses is also tunable by turning on/off each unit pulse generator cell.

Fig. 6. Block diagram of the proposed digital pulse generator.

3 Measurement results

The UWB RF transceiver is implemented on 0.18 μm CMOS technology and measured. The on/off keying (OOK) with 1 Mbps RZ data is used for the transmitter modulation input. Fig. 7 shows the measured output power spectrums of the UWB transmitter for each three band compliant with FCC mask in 3 ~ 5 GHz band. The carrier frequency is changed from 3.5 GHz to 4.5 GHz by tuning the delay cell current. All of them meet the FCC spectrum density requirement of -41.3 dBm/MHz . Since the transmitter is used for the noncoherent energy detection receiver, the carrier frequency accuracy and the phase noise are not stringent and the finite digital frequency trimming is sufficient. The measured energy efficiency per pulse is 20.6 pJ/bit, while excluding driver amplifier power consumption.

Fig. 7. Measured power spectrum of the UWB transmitter (three bands).

The measured RF performance of the receiver circuit blocks such as LNA gain and NF cannot be measured directly in the RF chip. Even though the measured results of the RF front end are absent here, we present the measured sensitivity and the sensitivity improvement using the RF notch filter with 2.4 GHz CW interferer. The 2.4 GHz interferer is chosen because the 2.4 GHz WiFi noise is mostly influential in the actual environments and hard to be filtered out even with the external filter.

Fig. 8 shows the measured output voltage waveform at the receiver output, which is used directly for the digital modem input. The comparator output buffer circuit (not shown in Fig. 1) makes 25 ns-duration digital output data for the FPGA modem interface. Connecting to the digital modem part, the sensitivity of UWB receiver is measured to meet the required BER of 10^{-3} . To measure the sensitivity, the UWB pulse signal from the transmitter mounted on the other board is going through the attenuator and injected to the input of the receiver. The measured sensitivity is presented in Fig. 9. The hollowed triangles indicate the measured sensitivity without the 2.4 GHz interference.

The measured sensitivity ranges from -70.9 to -62.9 dBm for the

Fig. 8. Measured voltage waveform at the receiver output.

Fig. 9. Measured sensitivity improvement with RF notch filter.

desired frequency band. And the hollowed circles are the sensitivity when the -30 dBm 2.4 GHz CW interferer enters together and the RF notch filter is 'off'. Naturally, the sensitivity is degraded 17 dB in the worst case. On the other hand, the hollowed rectangles are the sensitivity with the RF notch filter 'on' and the sensitivity power is improved more than 10 dB compared with the case of RF notch filter 'off'. Since the blocking signal maximum limit below 2.5 GHz is 0 dBm and the frequency characteristics of the external RF BPF and the antenna are assumed, the interferer power of -30 dBm is reasonable.

For the smaller interferer power of -45 dBm or less, the RF notch filter is useless because there is little difference in the sensitivity. For the interferer higher than -25 dBm, the sensitivity even with the RF notch filter is also degraded seriously due to the RF circuit saturation. Conclusively, the jamming signals around $-25 \sim -40$ dBm can be alleviated significantly below 2.4 GHz with the aid of the integrated RF notch filter.

The current consumption of the RF receiver and transmitter are 27.5 mA and 25.5 mA (including DA) at the 1.8 V supply, respectively.

Table I gives the summary of the measured performance and a comparison with previously published papers. Fig. 10 shows the photograph of the fabricated UWB RF transceiver chip. The chip is implemented on the $0.18\mu\text{m}$ CMOS technology. The chip size of the UWB RF receiver is $2.5\text{ mm} \times 2.6\text{ mm}$.

Table I. Performance comparison of IR-UWB transceiver.

		[1]	[2]	[3]	[4]	This work
Technology		BiCMOS $0.18\mu\text{m}$	CMOS $0.13\mu\text{m}$	CMOS $0.18\mu\text{m}$	CMOS $0.18\mu\text{m}$	CMOS $0.18\mu\text{m}$
Operating frequency		3.1~10.6GHz	4~5GHz	3~5GHz	3.25~4.75 GHz	3~5 GHz
Modulation		BPSK	DBPSK	OOK	BPSK	OOK
Data rate		100Mbps	31Mbps	1Mbps	1Gbps	1Mbps
Unwanted band rejection		10 dB	N/A	N/A	N/A	15 dB
Sensitivity improvement		N/A	N/A	N/A	N/A	> 10dB
Sensitivity@BER 10^{-3}		-80dBm	-78dBm	-88dBm	N/A	- 65 dBm
Power efficiency @1Mbps	Tx	N/A	0.7nJ/bit	0.3nJ/bit	108nJ/bit	20.6 pJ/bit (excluding DA)
	Rx	53.7nJ/bit	7nJ/bit	4.3nJ/bit	98nJ/bit	49.5nJ/bit
Chip size		2.3 mm^2	8 mm^2	12 mm^2	15 mm^2	6.5 mm^2

Fig. 10. Photograph of the fabricated UWB RF transceiver chip.

4 Conclusion

In this paper, a fully integrated 3 ~ 5 GHz IR-UWB transceiver chip is realized on $0.18\mu\text{m}$ CMOS technology. The low power digital impulse generator with the bandwidth and frequency tenability is designed compliant with FCC regulation. The energy efficiency of transmitter excluding DA is 20.6 pJ/bit. The receiver current consumption is 27.5 mA. The measured receiver sensitivity is -65 dBm at 4 GHz and the integrated RF notch filter enhances the sensitivity more than 10 dB even with -30 dBm interferer at 2.4 GHz band, which effectively improves the performance of the UWB transceiver chip in the actual noisy environment.

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