3D Networks-on-Chip mapping targeting minimum signal TSVs

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Abstract: The sharply increased complexity of multi-core systems has motivated the architecture of Networks-on-Chip (NoC) to evolve from 2D to 3D. With the objective of optimizing 3D NoC system for specific applications, a new mapping scheme with the goal of reducing signal TSVs and peak temperature is proposed in this paper. The interlayer communication is optimized, which facilitates reduction of signal TSVs. What’s more, the peak temperature is limited by placing IP cores with high power on the layer close to the heat sink. Experimental results indicate that the number of signal TSVs is decreased and that tradeoffs can be made between the number of signal TSVs and peak temperature.

Keywords: Networks-on-Chip, 3D, mapping, TSV
Classification: Integrated circuits

References

1 Introduction

With the continuous growing number of transistors, the high complexity and increasing area of chips have led to more challenges in conventional NoC architecture. Maintaining the system performance and density of transistors on chips, NoC is evolving from 2D to 3D. What’s more, 3D NoC which stacks several active layers vertically also brings in the advantages of low vertical link latency and low power overheads with signal Through Silicon Vias (TSVs) delivering packets. But there are also new challenges in 3D NoC. First, the stack of layers makes it more difficult for heat to dissipate and this fact results in severe thermal problems. Second, the low yield of signal TSVs has a great impact on the yield of the whole chip [1]. To solve these problems, designers map applications onto different topologies with the specific objectives. There have been several works on mapping during 3D NoC synthesis. P. K. Hamedani, et al. investigated three different mapping algorithms to explore the thermal constraints and their effects on temperature and performance of 3D NoC [2]. J. Wang, et al. presented a latency-aware mapping algorithm for 3D NoC which took the packet latency not only under no congestion but also under congestion into account in [3]. With the objective of avoiding suboptimal designs during mapping, N. Kapadia and S. Pasricha [4] suggested a novel PDN-aware 3D NoC synthesis framework to optimize the performance of systems. Unfortunately, during 3D NoC mapping, previous works ignored the reduction of signal TSVs can benefit from the reduction of inter-layer communication.

In this paper, we propose a new mapping scheme which maps IP cores to symmetric 3D Mesh. Different from previous works, we will reduce inter-layer communication to minimize the number of signal TSVs which are responsible for packets delivering and heat dissipation, leaving more unused TSVs to be thermal TSVs which are only for heat dissipation. Obviously, the number of signal TSVs impacts the yield of chips much more than that of thermal TSVs, thus the reduction in signal TSVs benefits the yield of the chip a lot. There are two main steps in this method, mapping IP cores to symmetric 3D Mesh and specifying the distribution of signal TSVs. During the mapping of IP cores, IP cores with different tasks will be assigned to different nodes in symmetric 3D Mesh. We accomplish this step with two sub-steps, inter-layer mapping and intra-layer mapping.

2 Problem formulation

Mapping IP cores to symmetric 3D Mesh architecture is a process which assigns each IP core one position on the architecture to achieve optimized systems. Since the distribution of signal TSVs varies with the specific application in our scheme, the step which determines the distribution of signal TSVs is also needed.
2.1 Definition

Definition 1: An application core graph is a weighted directed graph $ACG(V,E)$, where $V$ is a set of IP cores and $E$ is a set of communications. Each directed edge $e_{i,j} \in E$ denotes that there exists communication from IP core $v_i \in V$ to IP core $v_j \in V$, and the weight $\omega_{i,j}$ of the edge $e_{i,j}$ denotes the communication volume from IP core $v_i \in V$ to IP core $v_j \in V$.

Definition 2: A 3D NoC architecture graph is an undirected graph $NAG(N,T)$, where $N$ is a set of nodes, and $T$ is a set of TSVs including signal TSVs and thermal TSVs. The position of one node $n_i \in N$ is specified with the coordinate $(x_i, y_i, z_i)$, and the position of one TSV $t_i \in T$ is defined as $(l_{1i}, l_{2i}, x_i, y_i)$ in which $l_{1i}$ and $l_{2i}$ denote the two layers which the TSV connects and $l_{1i} < l_{2i}$, $x_i$ and $y_i$ denote the $x$ and $y$ coordinates. Since high bandwidth can be achieved in symmetric 3D Mesh, we choose symmetric 3D Mesh as the target architecture for mapping. Fig. 1 describes the architecture of symmetric 3D Mesh and the definition of the positions in detail.

![Symmetric 3D Mesh architecture](image)

Fig. 1. Symmetric 3D Mesh architecture.

Given the two definitions above, mapping IP cores to the 3D NoC architecture can be described as one problem that how to map each IP core $v_i \in V$ in the $ACG$ to one node $n_i \in N$ in the $NAG$ to achieve the optimized objectives. After mapping, the positions of signal TSVs should be determined in the $NAG$ to support communication in the vertical direction.

2.2 Optimization model

Traffic in the vertical direction flows through signal TSVs, there must be enough signal TSVs to meet the constraint of bandwidth. Also, Thermal problem is one concern in 3D NoC architecture. In the proposed mapping scheme, we focus on the optimization of the number of signal TSVs and peak temperature in NoC. However, the objectives of minimizing the number of signal TSVs and peak temperature may conflict during mapping. Based on this, we build the optimization model as

$$f(M_{\text{inter}}) = \min \left\{ \alpha \times \frac{ST_{\text{num}}}{ST_{\text{num}}_{\text{min}}} + \beta \times \frac{T_p}{T_{p_{\text{min}}}} \right\}$$  \quad (1)$$

where $M_{\text{inter}}$ is one mapping result, $ST_{\text{num}}$ and $T_p$ denote the number of signal TSVs and peak temperature, $ST_{\text{num}}_{\text{min}}$ and $T_{p_{\text{min}}}$ denote the mini-
mum number of signal TSVs and minimum peak temperature respectively, $\alpha$ and $\beta$ are the weighting coefficients of two objectives and $\alpha + \beta = 1$. Different levels of optimization can be obtained by adjusting the two coefficients.

It can be concluded that the reduction of signal TSVs depends on the reduction of inter-layer traffic. The model of the number of signal TSVs is given by

$$ST_{num} = \sum_{i=1}^{num} \sum_{j=1}^{num} C_{i,j} \times |i-j|$$

(2)

where $num$ denotes the number of layers in NoC, $C_{i,j}$ denotes the communication volume from the $ith$ layer to the $jth$ layer.

To obtain the peak temperature of the chip, the thermal model in HotSpot [5] is introduced in our method. This model is built as

$$\begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_n \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} & \ldots & \ldots & R_{1n} \\ R_{21} & R_{22} & \ldots & \ldots & R_{2n} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ R_{n1} & R_{n2} & \ldots & \ldots & R_{nn} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_n \end{bmatrix}$$

(3)

where $P_i$ is the power consumed by IP core $v_i$, $T_i$ is the temperature of IP core $v_i$, $n$ is the number of IP cores, and $R_{ij}$ denotes the thermal resistance between IP core $v_i$ and $v_j$. Then, the peak temperature is given as

$$T_p = \max\{T_i|i = 1, 2, 3 \ldots n\}$$

(4)

3 Mapping

As is described above, inter-layer mapping will be carried out first. IP cores will be assigned to different layers during this stage with the objective of minimizing the number of signal TSVs and peak temperature. The search for optimized inter-layer mapping is completed with the simulated annealing engine. Perturbation is done to the current inter-layer mapping result. Whether the perturbation is accepted depends on the performance of the obtained new mapping result and the current temperature. After cooling operation and enough iterations, the optimal solution will be achieved. Pseudo code for inter-layer mapping is shown in Fig. 2 (a). After specifying the layer each IP core is assigned to, intra-layer mapping who decides the exact node each IP core matches is executed targeting minimum total communication cost. We also use the simulated annealing engine to optimize intra-layer mapping. Different from inter-layer mapping, new mapping result is created by randomly change the positions of two IP cores on the same layer.

At this point, we have mapped all IP cores in one specific application to the nodes in symmetric 3D Mesh. During the next stage, distribution of signal TSVs is specified to support communication in the vertical direction.

To build vertical paths for inter-layer communication with signal TSVs, we place signal TSVs for each inter-layer traffic flow at the positions which
are closed to the communicating IP cores targeting minimum communication cost. Traffic flows in the specific application will be checked one by one. The \( x \) and \( y \) coordinates of the signal TSVs will be the same as those of the source IP core. For example, when IP core \( v_i(x_i, y_i, z_i) \) sends packets to IP core \( v_j(x_j, y_j, z_i + 1) \), signal TSVs will be specified at \( (z_i, z_i + 1, x_i, y_i) \), and when IP core \( v_i(x_i, y_i, z_i) \) sends packets to IP core \( v_j(x_j, y_j, z_i + 2) \), signal TSVs will be specified at \( (z_i, z_i + 1, x_i, y_i) \) and \( (z_i + 1, z_i + 2, x_i, y_i) \). Based on such distribution of signal TSVs, packets can be routed to the destination node with ZXY routing, which is definitely deadlock free. What’s more, the distribution of signal TSVs also ensures that each traffic flow is delivered by specified TSVs so that different traffic flows will not share TSVs to avoid contention. These all ensure the system performance.

4 Experimental results

Setting up the experiments, we implement the algorithms in C++ language. To obtain the impacts on the number of signal TSVs, we set \( \alpha = 1 \) and \( \beta = 0 \) in the objective model \( f \). Eight applications including PIP, MWD, MPEG4, VOPD, and four randomly generated applications (M1-M4) are tested to check whether the improvement can be achieved by the proposed method. The application information and the size of relevant 3D NoC architecture are listed in Fig. 2 (b).

![Algorithm Inter_layer_mapping(T,Tinv=ACGG(V,E))](image)

**Algorithm Inter_layer_mapping(T,Tinv=ACGG(V,E))**

Input:Initial temperature

- \( T_{min} \): minimum temperature
- \( ACGG(V,E) \): application core graph

Output:\( M_{opt} \)

1: randomly generate one inter-layer mapping result \( M \)
2: current result = \( M \)
3: while(\( T>T_{min} \))
4: \( M \) = randomly choose two IP cores
5: while(\{two IP cores are on the same layer in \( M \}\})
6: change their positions, obtain \( M' \)
7: if \( f(M) < f(M') \) then
8: current result = \( M' \)
9: else
10: current result = \( M \)
11: end if
12: end while
13: end while
14: return \( M_{opt} \)

![Fig. 2.](image)

Fig. 2. (a) Pseudo code for inter-layer mapping. (b) Application information. (c) Evaluation of the number of signal TSVs.

Fig. 2 (c) depicts the comparison of the number of signal TSVs in the scheme targeting minimum signal TSVs to that in one random mapping case. From experimental results, the number of signal TSVs is average decreased by 65.27\%. Based on current packaging technology, the failure rate of one single TSV ranges between \( 10^{-5} \) and \( 10^{-4} \) [6]. The proposed method achieves an average 8.9\% increase in the yield of chips.

In order to make it clear that whether the coefficients in \( f \) can achieve a
tradeoff between the number of signal TSVs and peak temperature, we adjust the values of $\alpha$ and $\beta$ to obtain the mapping results targeting only minimum signal TSVs (OMT case), or only minimum peak temperature (OPT case), or both the two objectives (hybrid case). To calculate the peak temperature, a random power density is assigned to each IP core. The range of random power is between $10 \text{ W/cm}^2$ and $60 \text{ W/cm}^2$ [2], which is a typical value in modern circuits under the technology of 45 nm. Fig. 3 shows the variation of the number of signal TSVs and peak temperature with these three objectives for various applications. From the figure, we can see that the hybrid case achieves a 67.499% decrease in the number of signal TSVs, that is, a 4.93% increase in the yield of chips compared with the case targeting minimum peak temperature and a 6.1% decrease in peak temperature compared with the case targeting minimum signal TSVs at most. It can be concluded that tradeoffs have been achieved by our method.

Fig. 3. (a) The number of signal TSVs and (b) peak temperature under different objectives.

5 Conclusion

In this paper, we propose a method which maps specified applications to symmetric 3D Mesh. The system is optimized during inter-layer mapping, intra-layer mapping and signal TSV distribution design stages. Introducing in the uneven distribution of signal TSVs, this idea decreases the number of signal TSVs by minimizing inter-layer communication. Meanwhile, in our design scheme, the peak temperature is also decreased.

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