Low-power and area-efficient 9-transistor double-edge triggered flip-flop

S. Muthukumar\textsuperscript{a)} and GoangSeog Choi\textsuperscript{b)}

Department of Information and Communication Engineering, Chosun University, 309, Pilmoon-daero, Dong, GwangJu, 501–759, Korea

\textsuperscript{a)} muthukumar9167@gmail.com
\textsuperscript{b)} gschoigs@chosun.ac.kr

Abstract: Double-edge triggered flip-flops offer a solution to clock power reduction by lowering the clock frequency and maintaining the same data rate. A compact 9-transistor double-edge triggered flip-flop for reducing flip-flop power is proposed. A combination of a selective swing-based partial transmission gate (TG) approach and multi-\textit{V}_t transistors is used to make it area and power-efficient. The selective swing-based transmission gate approach reduces the transistor count, and the selective use of low-\textit{V}_t transistors overcomes the effect of any intermediate low swing voltage levels in the circuit due to a partial TG approach. Low transistor count reduces capacitive load of the dynamic power component, and selective use of low-\textit{V}_t transistors improves circuit performance as well as reduces power-delay product. The proposed circuit is implemented in the Samsung 130 nm 1P6M Multi-\textit{V}_t CMOS process technology and simulated for various PVT conditions. Results show that the power consumption of the circuit is reduced by 9.58\% and energy reduced by 14.2\% with a 5.12\% improvement in speed for a slow process when compared to the previous techniques.

Keywords: DETFF, low-\textit{V}_t, XOR, clock power

Classification: Integrated circuits

References

1 Introduction

The clock is one of the most important signals in processors and synchronous circuits of any kind. In designs with a large clock network, clock power consumption typically varies from 20 to 40% of the total dynamic power consumption of the chip [1, 2]. There are lots of clocking techniques or distribution types proposed to reduce power consumption. Other ways of reducing clock power is to lower the clock frequency without disturbing the data rate by using double-edge triggered flip-flops (DETFFs). DETFFs will yield good power savings in designs where a low signal-to-clock ratio exists. Clock frequency can be reduced to half using DETFFs (and hence, the dynamic power reduced to half) while maintaining the same throughput for the design. In large clocked networks, flip-flop burns up nearly 20% of total dynamic power consumption. Using DETFFs in clocked networks will reduce clock frequency, and hence the dynamic power, to half for the same data throughput as discussed in [3]. Many techniques had been proposed earlier for saving clock power and also for saving flip-flop power. They proposed low swing clock drivers to reduce clock power and eliminate redundant transitions at internal nodes of the flip-flop [5, 6] to reduce dynamic power. But the power savings were not as expected due to high transistor count, which brings capacitive load. Parallel-connected dual latch type low power DETFFs with pass transistor logic (PTL) switches [7] and TG switches [8] overload the clock driver and occupy more space. Another dynamic DETFF proposed by Hossain, Wronski and Albicki [7] has the drawback of being affected by crosstalk due to its internal floating node in hold mode. Blair [9] proposed a low-power DETFF similar to Hossain’s configuration [7], replacing the inverter in the feedback loop with a weak pull-up transistor. The circuit is static for holding data high, but not static for holding data low in the internal node, which results in weak noise immunity and also offers more clock-to-Q delay. Another low-power approach [10] similar to that of [7], a mix-up of static and dynamic logic, has the drawback of driver overload and low speed.

Wu and Wei’s low power architecture [11] has poor delay performance...
due to the AND operation of the clock, with its delayed clock signal in the sampling path nearly \(5t_{\text{inv}} + t_{\text{pass\_switch}}\) including two inverters in the data path. Also it offers unbalanced loading to the input signal. The low-power DETFF proposed by Strollo, Napoli, and Cimino [12] is compact and proves to have high dynamic power savings. Even though it has good power savings, its delay performance is as poor as \(4t_{\text{inv}} + t_{\text{pass\_switch}}\), similar drawbacks also observed in [13]. Also, it is not fully static in nature; the internal node x is floating when holding low data, so it is more sensitive to crosstalk. Even though the above discussed techniques reduce a considerable amount of dynamic power, those techniques have any one of many shortcomings, such as complex circuitry, more transistor count (which occupies a large area), low speed/low data throughput, and crosstalk effects. So we need a static DETFF that is power-efficient as well as area-efficient with high-speed performance.

Johnson and Kourtev [14] introduced a simple and power-efficient static DETFF, as shown in Fig. 1 (a). The basic operation is performing an exclusive-OR of the clock and its delayed inverted signal CLKX ⊕ CLKY where the low output will turn on the pMOS pass switch to latch the data at D input. The XOR output is always a constant logic 1, except for a very short duration. It goes to logic 0 for a very short duration due to the delay encountered by CLKY changing its value in response to the change in the CLKX signal, as illustrated in Fig. 1 (b). A modification to the above to further reduce its power consumption and improve its speed was proposed by Sung and Chang [15] as shown in Fig. 2. All the transistors in the design, including clock driver circuits (except those in the back-to-back inverter of Johnson and Kourtev [14]) were replaced by low-\(V_t\) transistors, and a low swing driver was adapted to reduce the power consumption and to reduce the leakage current issue. Later this approach was modified again by Wang [16] as shown in Fig. 3, highlighting the large area, standby sub-threshold leakage current, and weak noise immunity issues of using low-\(V_t\) transistors in the design [15].

![Fig. 1. (a) Proposed DETFF from Johnson and Kourtev [14]; (b) Clock timing and XOR gate output waveform](image-url)
which also reduces the transistor count by one. The operation of the DETFF is explained in Section 2. Section 3 explains its implementation and tabulates its performance in comparison with other architectures. Section 4 concludes with the advantages of our architecture based on its results.

2 Proposed DETFF

A full swing clock driver circuit as shown in Fig. 4 (a) is used to trigger the DETFF. A Pass Transistor Logic (PTL)-based XOR gate is implemented using CLXX, CLKY, and CLKZ, which performs XOR of the clock signal and its delayed inverted signal CLXX ⊕ CLKY as shown in Fig. 4 (a). The XOR output at node x is always logic 1 because the operation is between the signal and its complement. But for a short duration, both signal and its complement will be the same value, as the change in CLXX will propagate through three inverters to make the corresponding change at CLKY. So the XOR output will go to logic 0 for a very short duration (3tinvp approximately). This will happen at both the rising and the falling edge of clock signal CLXX as illustrated in Fig. 1 (b). In Fig. 4 (a), the logic low at node x will turn on the pMOS pass switch M5 to latch the data at input port D. In this way, the data is latched at both the edges of the clock signal.
The PTL-based XOR of Fig. 4 (a) had a drawback of low swing ($V_{tp}$ to $V_{dd}/C_0 V_{tn}$). Let us discuss the effects of low swing in the circuit of Fig. 4 (a) in the following subsection 2.1 and 2.2 in detail.

### 2.1 Latching period

At the time of latching, node x is at $V_{tp}$.

**Case 1:** If data input is logic 0 and voltage at node y in the holding loop is at logic 1, then node y will go to $2V_{tp}$ instead of 0 V. If the operating voltage of the design is high, then $2V_{tp}$ is much lower than $V_{dd}/2$, so inverter $I_1$ pushes its output close to $V_{dd}$ (by proper sizing), which will drive inverter $I_2$, which is driving the node y nothing but inverter $I_1$ during the non-latching period. During the non-latching period, voltage at node y will be restored to 0 V by the regenerative property of the back-to-back inverters connected through an nMOS switch (M6). But this will not be the case if the operating voltage is low (1 V or 1.2 V); $2V_{tp}$ is nearly equal to $V_{dd}/2$; even though it can be solvable by sizing the inverters, it will need a long time for restoration, which will increase the short circuit current in the back-to-back inverters and, hence, the power consumption. Also, sizing will increase the size of certain transistors in inverters $I_1$ and $I_2$, which increases capacitive loading and increases the latching time, which in turn requires sizing of clock drivers to increase the logic low duration of the XOR gate.

**Case 2:** When the data input, D is logic 0 and voltage at node y is logic 0, there will be no issue as discussed earlier in Case 1 because the previously held data are the same as the new data to be latched.

**Case 3:** If the data input is logic 1, irrespective of the value at node y, the input data is latched without any problems due to the good pull-up property of the pMOS switch, M5.

To overcome the problem discussed in Case 1, PTL-based XOR of Fig. 4 (a) is partially replaced by TG logic-connecting M3 as shown in Fig. 4 (b).

### 2.2 Holding period

During the hold period of the flip-flop, output of the XOR at node x of Fig. 4 (a), which is at ($V_{dd} - V_{tn}$) V, will turn on the nMOS switch (M6),
which connects the back-to-back inverter I₁ and I₂ to hold the latched data until the next clock edge. nMOS is a weak 1 and a good 0 switch; even though its gate voltage is $V_{dd} - V_{tn}$, there is no problem in holding the logic 0 state because it is permanently ON. But there may be a problem in holding logic 1. Let us discuss this in detail.

Assume that flip-flop latches logic 1 and now the circuit goes to hold mode; at that instant, node y & $Q$ are at logic 1 ($V_{dd}$), and the nMOS ($M₀$) is ON. Both ends of the nMOS switch are at $V_{dd}$. But node y is floating, so there will be a charge leakage; it will not be a problem if the DETFF is used in high-speed design. But when the circuit is in standby mode due to clock gating or some other techniques, voltage at node y will drop. The node is restored by I₂ through the nMOS ($M₀$) switch, but nMOS is a weak 1 switch, so as per switch property, it can restore the node up to $V_{dd} - 2V_{tn}$. This will be the case also for Johnson and Kourtev [14], Sung and Chang [15], and Wang [16], but they used a full swing XOR gate, so the corresponding node in those circuits is restored to $V_{dd} - V_{tn}$. As per the above discussion, if node y in Fig. 4 (a) is restored only to $V_{dd} - 2V_{tn}$ then it may raise problems like more short circuit current in I₁. Transistor sizing can avoid undesirable output at $\bar{Q}$ and $Q$, similar to the discussion in case 1. Actually, there is no such problem as we discussed above. Even though the voltage at node y drops during hold mode or in standby, the subthreshold leakage current maintains its value close to $V_{dd}$, ensuring $Q$ and $Q$ are at the desired value. To speed up the voltage restoration by increasing the subthreshold leakage current, transistor $M₀$ of Fig. 4 (a) is replaced by a low-$V_t$ transistor as shown in Fig. 4 (b). Also to improve the swing of the XOR output, transistors $M₃$ of the proposed DETFF (Fig. 4 (b)) is replaced by a low-$V_t$ transistor. Finally, a low swing 3-transistor partial TG-based XOR gate is used in the proposed DETFF to minimize the area and clock driver load to reduce the clock power, as well as flip-flop power. To improve its speed, transistor $M₁$ and $M₂$ of the XOR gate are replaced by low-$V_t$ transistors, and transistors in the critical path $M₅$ and $M₇$ are replaced by low-$V_t$ transistors [4] as shown in Fig. 4 (b). Increase in area due to low-$V_t$ transistors [16] is compensated by a 3-Transistor XOR gate instead of 4 transistors. Application of low-$V_t$ transistors may account for increase in leakage power but overall it helps in maintaining the functionality of DETFF and reduces its dynamic power. The dynamic power reduction percentage is comparatively higher than the increase in leakage power. Overall, considerable power savings is achieved by the proposed DETFF, which is discussed in detail in Section 3.

3 Implementation and simulation results

The proposed design was implemented in Cadence Virtuoso ADE and simulated for all the process corners in HSPICE using Samsung 130 nm (1P6M) Multi-$Vₜ$ CMOS process technology. PVT conditions adopted for the simulation are listed in Table I and threshold voltage of the MOS device in the multi-$Vₜ$ process is listed in Table II.

The layout of the proposed DETFF shown in Fig. 5 is developed in Virtuoso Layout Editor and post-layout simulation is carried out in HSPICE. The DETFF is simulated for the “01” and “10” sequence to
calculate the dynamic power; all possible conditions are considered for leakage power calculation, and its average is tabulated. To show individual and system performance, we implemented a 4-bit synchronous counter and simulated the same. The counter is simulated for one complete count to measure the dynamic power. The clock frequency applied for all the simulations is 250 MHz. The performance comparison of the proposed design with previous works [15, 16] is shown in Table III. Table IV shows the system performance.

Table I. PVT conditions for simulation

<table>
<thead>
<tr>
<th>Process Corner</th>
<th>Voltage(V)</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>1.32</td>
<td>-55</td>
</tr>
<tr>
<td>SS</td>
<td>1.08</td>
<td>125</td>
</tr>
<tr>
<td>TT</td>
<td>1.20</td>
<td>70</td>
</tr>
<tr>
<td>SF</td>
<td>1.32</td>
<td>-55</td>
</tr>
<tr>
<td>FS</td>
<td>1.32</td>
<td>-55</td>
</tr>
</tbody>
</table>

Table II. Threshold Voltage of Samsung 130 nm Multi-V_t CMOS process technology for V_dd = 1.2 V and W/L = 0.3/0.13

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Model</th>
<th>V_t (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TT</td>
<td>SS</td>
</tr>
<tr>
<td>PMOS</td>
<td>Normal-V_t</td>
<td>-374</td>
</tr>
<tr>
<td></td>
<td>Low-V_t</td>
<td>-293</td>
</tr>
<tr>
<td></td>
<td>High-V_t</td>
<td>-483</td>
</tr>
<tr>
<td>NMOS</td>
<td>Normal-V_t</td>
<td>421</td>
</tr>
<tr>
<td></td>
<td>Low-V_t</td>
<td>360</td>
</tr>
<tr>
<td></td>
<td>High-V_t</td>
<td>552</td>
</tr>
</tbody>
</table>

Fig. 5. Layout of the proposed DETFF - (12.5 x 2.37) μm²
Replacement of high drive strength inverter for $I_1$ and $I_2$ in Fig. 2 [16] which is discussed above for the FS process corner simulation will vary the power and performance parameters accordingly and make it not suitable for comparing it with [16] and [P], as these architectures have no such requirement for the above said process conditions. So those results are not tabulated and compared. The performance comparison in [16] shows that Wang’s DETFF [16] is energy efficient than Sung’s DETFF [15]. So let us focus our discussion between [16] and our proposed DETFF.

Table III. Performance comparison of proposed DETFF with other DETFF circuits

<table>
<thead>
<tr>
<th>PC</th>
<th>Atech</th>
<th>$t_{AC}$ (ps)</th>
<th>$t_{AH}$ (ps)</th>
<th>$P_{IN}$ (µW)</th>
<th>$P_{OUT}$ (µW)</th>
<th>$P_{TT}$ (µW)</th>
<th>$P_{SS}$ (µW)</th>
<th>$P_{PS}$ (µW)</th>
<th>$P_{SH}$ (µW)</th>
<th>PDP (F)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>[16]</td>
<td>-5.0</td>
<td>147</td>
<td>3.9</td>
<td>4.65</td>
<td>24.08</td>
<td>0.47</td>
<td>27.98</td>
<td>5.12</td>
<td>147</td>
</tr>
<tr>
<td></td>
<td>Our’s [P]</td>
<td>-4.7</td>
<td>142</td>
<td>4.14</td>
<td>3.41</td>
<td>20.61</td>
<td>0.47</td>
<td>24.75</td>
<td>3.88</td>
<td>142</td>
</tr>
<tr>
<td></td>
<td>[16]</td>
<td>-19.1</td>
<td>393</td>
<td>2.04</td>
<td>1.11</td>
<td>15.61</td>
<td>4.18</td>
<td>17.65</td>
<td>5.29</td>
<td>393</td>
</tr>
<tr>
<td></td>
<td>Our’s [P]</td>
<td>-8.5</td>
<td>373</td>
<td>2.52</td>
<td>1.01</td>
<td>13.44</td>
<td>4.18</td>
<td>15.96</td>
<td>5.19</td>
<td>373</td>
</tr>
<tr>
<td>TT</td>
<td>[16]</td>
<td>-10.3</td>
<td>238</td>
<td>2.59</td>
<td>3.21</td>
<td>19.54</td>
<td>5.41</td>
<td>22.53</td>
<td>8.62</td>
<td>238</td>
</tr>
<tr>
<td></td>
<td>Our’s [P]</td>
<td>-8.29</td>
<td>227</td>
<td>3.37</td>
<td>3.41</td>
<td>16.75</td>
<td>5.41</td>
<td>20.12</td>
<td>8.82</td>
<td>227</td>
</tr>
<tr>
<td>SF</td>
<td>[15]</td>
<td>-5.94</td>
<td>166</td>
<td>15.36</td>
<td>21.12</td>
<td>23.09</td>
<td>2.84</td>
<td>38.45</td>
<td>23.96</td>
<td>161</td>
</tr>
<tr>
<td></td>
<td>[16]</td>
<td>-7.75</td>
<td>165</td>
<td>3.92</td>
<td>1.18</td>
<td>23.11</td>
<td>0.27</td>
<td>27.03</td>
<td>1.45</td>
<td>165</td>
</tr>
<tr>
<td></td>
<td>Our’s [P]</td>
<td>-5.04</td>
<td>160</td>
<td>4.26</td>
<td>0.08</td>
<td>19.78</td>
<td>0.27</td>
<td>20.04</td>
<td>0.35</td>
<td>160</td>
</tr>
<tr>
<td>FS</td>
<td>[16]</td>
<td>-6.56</td>
<td>203</td>
<td>3.66</td>
<td>3.311</td>
<td>23.43</td>
<td>0.27</td>
<td>27.09</td>
<td>3.58</td>
<td>203</td>
</tr>
<tr>
<td></td>
<td>Our’s [P]</td>
<td>-5.02</td>
<td>197</td>
<td>3.96</td>
<td>3.25</td>
<td>20.13</td>
<td>0.27</td>
<td>24.09</td>
<td>3.52</td>
<td>197</td>
</tr>
</tbody>
</table>

Table IV. Comparison of a 4-bit counter including clock driver built with proposed DETFF and other DETFF’s

<table>
<thead>
<tr>
<th>Counter’s F/F type</th>
<th>Dynamic Power (µW)</th>
<th>Static Power (µW)</th>
<th>Delay (ps)</th>
<th>PDP (F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15]</td>
<td>105.77</td>
<td>21.82</td>
<td>364</td>
<td>38.5</td>
</tr>
<tr>
<td>[16]</td>
<td>92.23</td>
<td>34.59</td>
<td>363</td>
<td>33.5</td>
</tr>
<tr>
<td>Proposed [P]</td>
<td>83.61</td>
<td>35.37</td>
<td>347.8</td>
<td>29.1</td>
</tr>
</tbody>
</table>

Process = TT, $V_{DD} = 1.2$V, $T = 70$° C and Load = 10F

Even though power consumption of flip-flop circuit in Wang’s DETFF [16] is less compared to our proposed DETFF, load offered by our proposed DETFF to the clock driver circuit is less compared to [16]. So our proposed DETFF saves considerable amount of clock driver power which is dominant than power savings in flip-flop circuit. Performance comparison and analysis in Fig. 6 and 7 shows that the proposed DETFF saves around 11.54% of the total power at FF, 14.68% of the energy at TT, and provides a speed improvement of 5.12% at SS as compared to the previous...
Fig. 6. Performance comparison of the proposed DETFF with [15] and [16] (a) Total Avg. Dynamic Power (b) Rise Delay (c) Fall Delay and (d) Power Delay Product
approaches [16]. Also its utilization in synchronous design (4 bit counter) shows 9.3% power and 13.13% energy savings with 4.19% improvement in speed as compared to [16] – refer Table IV. All the compared architectures holds an advantage of negative setup time and the hold time requirement of our proposed DETFF is 5.12% less compared to that of [16] at SS. Table V shows that the proposed DETFF reduces area by 1.64%. Even though it is less, in a clocked design with large no. of flip-flops, the proposed DETFF will save more power, energy and space with considerable improvement in speed.

Another important consideration for proper operation of the DETFF is $3t_{\text{inv}}$ delay between CLKX and the inverted clock signal CLKY must be sufficient to permit the XOR gate to fully evaluate, to turn on the PMOS

Fig. 7. Percentage reduction in power, energy and delay of the proposed DETFF (a) with [16] and (b) with [15]

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Area ($\mu$m$^2$)</th>
<th>Excess area (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[16]</td>
<td>30.12</td>
<td>1.64</td>
</tr>
<tr>
<td>Proposed [P]</td>
<td>29.63</td>
<td>-</td>
</tr>
</tbody>
</table>

Table V. Area comparison of proposed DETFF [P] with [15] and [16]
device $M_5$, and to allow the input $D$ to charge/discharge the input to the inverter $I_1$ i.e. $3t_{\text{inv}} > t_{\text{clk-Q}}$. The amount of time necessary for these events to complete will differ depending on the technology and transistor sizes used. For a minimum transistor sizing ($W/L = 0.3/0.13$) & Samsung 130 nm (1P6M) Multi-$V_t$ CMOS process technology, it was determined that the following condition must be satisfied: $3t_{\text{inv}} > 469$ ps considering all the PVT variations. This limitation hence put forth our proposed DETFF can operate upto a maximum clock speed of 1 GHz only. In [16], the limitation for DETFF is $3t_{\text{inv}} > 535$ ps and can operate at a maximum clock speed of 900 MHz. To improve the speed, transistor sizing can be performed in order to reduce the $3t_{\text{inv}}$ delay requirement but it necessitates a trade-off between power, area and delay.

### 4 Conclusions

A low power and compact double-edge triggered flip-flop was proposed in this paper. The 9-Transistor DETFF comprises a low swing partial TG-based XOR gate, back-to-back inverters, hold and sample switch. The simulation results prove its power and energy-saving capability. Its delay performance shows that it is suitable for high-speed design close to gigahertz range.

### Acknowledgments

This study was supported by research fund Chosun University, 2012. GoangSeog Choi is a corresponding author.