A low-voltage CMOS MIN circuit with $3N + 1$ complexity and 10 mV/10 ns corner error

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Abstract: An 1.5 V CMOS voltage-mode MIN circuit with $3N + 1$ complexity and 10 mV/10 ns corner error is presented. The proposed approach uses a low impedance configuration to operate with low voltage supply requirements and without the need of low-voltage techniques with large area requirements. The basic cell and a LTA circuit prototype were simulated, fabricated and characterized using a double poly, three metal layers 0.5 μm CMOS technology from ON SEMI foundry.

Keywords: low complexity LTA, low voltage LTA, LTA filters

Classification: Integrated circuits

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1 Introduction

The voltage shrinking in modern CMOS technologies and the growing need to develop efficient and low cost portable devices have obligated to produce analog circuits who operate with narrow voltage headrooms and supply voltages less than twice the gate-source voltage of the MOS device [1]. This condition entails analog designers to use low-voltage methodologies, such as bulk-driven [1] and floating-gate transistors [2]. Unfortunately, those techniques exhibit large area requirements which is a major disadvantage since area reduction is a crucial trend in extensive non-linear signal processing tasks, including pattern recognition, classification algorithms, data compression, nonlinear filters and fuzzy systems, to name a few [3, 4]. One of the basic building blocks of those systems is the minimum detector (MIN). MIN circuit or “Loser-Takes-All” (LTA) circuit [5, 6, 7, 8, 9, 10, 11, 12, 13] consists of identifying the smallest input value among N external inputs. The LTA realizations whose size increases linearly with N are denoted as circuits with $O(N)$ complexity.

Typical analog LTA or MIN implementations base their performance in MOS transistors working on saturation, a condition that is notably affected by the reduction of rail voltages. In this sense, the use of circuits with low output impedance have become a useful strategy for designing circuitry with a reduced rail voltage without forego the benefits of using transistors in saturation regime [12, 13]. This strategy is used in this paper to develop an LTA circuit based on a low output impedance inverting stage, which can operate with a minimum voltage supply of $V_{DD} = V_{GS} + 2V_{DS}$. The proposed LTA circuit consist of a voltage-based processor with $3N + 1$ complexity.

Fig. 1. Basic cells. (a) Lazzaro's cell. (b) Proposed basic cell. (c) Open-loop diagram of the basic cell (unity-gain feedback in dashed line).

2 The proposed basic cell

The proposed basic cell is a folded version of the Lazzaro's cell of Fig. 1 (a). In this figure, the transistor M_{n1} and the input current I_{in} are substituted respectively by a PMOS transistor M_{p1} and the drain current of M_{n1} , as is shown into the dashed region of Fig. 1 (b). With this modification, the proposed cell presents input and output signals in voltage-mode, denoted respectively by V_{in} and V_o . Also, this configuration overcomes, without adding complexity, the large voltage supply requirement of the Lazzaro's cell caused by the two gate-source voltage drops of M_{n1} and M_{n2} connected in series, reducing the supply voltage from $V_{DD_{min}} \approx V_{GS_{M_{n1}}} + V_{GS_{M_{n2}}} + V_{sat_{I_{in}}}$ to $V_{DD_{min}} \approx V_{GS_{M_{n2}}} + V_{sat_{M_{p1}}} + V_{sat_{I_b}}$ with a voltage swing $V_{sw} \approx V_{DD} - V_{GS_{M_{n2}}} - V_{sat_{M_{p1}}} - V_{sat_{I_b}}$ (V_{sat} is the overdrive voltage). An LTA with similar topology was reported earlier in [6], however, it was a current-mode, binary implementation with transistors working in subthreshold regime.

The DC gain of the proposed cell is obtained by performing a small signal analysis without considering the body effect, resulting

$$V_o = \frac{-g_{m_{M_{n1}}}}{g_{m_{M_{p1}}} - \frac{1}{g_{m_{M_{n2}}}(r_{o_{M_{p1}}} || r_{o_{M_{n1}}})(r_{o_{M_{n2}}} || r_{I_b})}} V_{in} \approx - \left(\frac{g_{m_{M_{n1}}}}{g_{m_{M_{p1}}}} \right) V_{in} \quad (1)$$

where g_m is the gate-source transconductance, r_o is the MOS output resistance and r_{I_b} is the output resistance of I_b . From (1), the ratio $g_{m_{M_{n1}}}/g_{m_{M_{p1}}}$ establishes the gain of the cell. It can be around unity or even larger. Besides by performing, again, a small signal analysis the output impedance of the proposed cell is obtained:

$$R_{out} = \frac{V_o}{\Delta_i} = - \frac{1}{g_{m_{M_{p1}}} g_{m_{M_{n2}}} (r_{o_{M_{p1}}} || r_{o_{M_{n1}}})} \quad (2)$$

The stability of the cell is analyzed with the circuit of Fig. 1 (c), following the procedure presented in [14]. As can be noticed, the basic cell has two poles: the dominant p_x at node “x” that determines the bandwidth (BW) of

Table I. Aspect ratio of transistors and design details of Figure 1 (b).

Transistor	W (μm)	L (μm)	Element	Value
M_{p1}	45	1.5	V_{DD}	1.5 V
M_{n2}	50	1.5	I_b	100 μA
M_{n1}	15	1.5	C_C, C_L	2 pF, 20 pF

the cell, and the non-dominant p_y at node “y”. These poles are denoted by

$$p_x = \frac{1}{2\pi C_x (r_{oMp1} || r_{oMn1})} \quad (3)$$

$$p_y = \frac{g_{mMn2}}{2\pi C_y} \quad (4)$$

where C is the total capacitance at each node. Now, by assuming an unity gain from V_{in} to node “y” (source follower configuration) and by neglecting the body effect, the open loop gain from V_{in} to V_{out} (without the connection of the dashed line) and the gain-bandwidth product result

$$|A_o| = g_{mMp1} (r_{oMp1} || r_{oMn1}) \quad (5)$$

$$GBW = |A_o|p_x = \frac{g_{mMp1}}{2\pi C_x} \quad (6)$$

Here, to guarantee stability is required $p_y \geq 3GBW$ or equivalently

$$C_x \geq 3 \frac{g_{mMp1}}{g_{mMn2}} C_y \approx \frac{1}{k} C_L \quad (7)$$

where $C_y \approx C_L$ (the load capacitance) and k is typically in the range from 5 to 10 because off $g_{mMn2} > g_{mMp1}$. This way, to guarantee stability is required a compensation capacitor C_C in node “x”.

3 Simulations and experimental results of the basic cell

The simulations of the basic cell were performed using HSpice and the parameters of a double-poly, three metal layers, 0.5 μm CMOS technology from ON-Semi foundry, with threshold voltages $V_{THN} = 0.69 V$ for NMOS and $V_{THP} = -0.98 V$ for PMOS. The aspect ratio of transistors and other design details are shown in Table I. A low frequency ramp was used as the input of the fabricated prototype to emulate a DC sweep in order to determine the DC working range. The result is depicted in Fig. 2. As can be observed, a working range of almost 0.5 V is appreciated. Besides, the step response of the basic cell was simulated with a load of $C_L = 20 pF$ and with an input square-wave signal of 2.5 MHz. Rise and fall times of 5 ns and 8 ns were obtained. The AC simulated and measured responses were realized with a DC input of 1.1 V, $C_L = 20 pF$ (to include the loading effect of the oscilloscope probes), and $C_C = 2 pF$. The simulated and measured bandwidths were respectively 17.8 MHz and 13 MHz, both with 2 dB overshoot. The discrepancy is due to parasitic effects associated with the PCB. Finally, the linearity of the system

Fig. 2. Measured working range of the proposed basic cell.

Fig. 3. Proposed LTA circuit based on a nested network.

was characterized by mean of the Total Harmonic Distortion (THD), which was measured experimentally using a center frequency of 300 kHz with signal amplitude of 100 mV and 1 V offset. It resulted 1.05% .

4 Proposed MIN circuit

A frequently used technique to obtain an MAX or “Winner-Takes-All” (WTA) circuit is by shortcutting the output nodes of voltage follower cells [5], which is referred as a nested voltage-follower network [7]. Since node outputs present typically low impedance, the cell with the highest input value will source/sink the highest current in order to be followed at the output. The MIN or LTA circuit is obtained by performing a Morgan operation to the WTA circuit. Based on this approach, several MIN/MAX circuits have been reported in the literature [5, 7, 12, 13]. Also based on this approach, a three input MIN circuit is proposed in this section. It is realized by using three of the inverting low-output impedance basic cells of Fig. 1 (b) with their output nodes shorted, as depicted in Fig. 3. In this circuit, $M_{xi,j}$ represents the i -th tran-

sistor of the j -th voltage follower cell, and x can be n or p . The output is the voltage V_o . Alternatively, it is possible to add a DC level shifter, which is conformed by the transistor M_{off} and the bias current source I_{b1} . In this case the output voltage is V_{o1} . I_{b1} and the aspect ratio of this transistor can be calculated to obtain an appropriate $V_{GS_{M_{off}}}$ value in order to reduce the systematic offset voltage between the DC level of the inputs and the DC level of V_{o1} . The operation of the DC level shifter can be analyzed as follows. Suppose that V_{in1} is the minimum of the three inputs. In consequence, the drain nodes of $M_{n1,2}$ and $M_{n1,3}$ has low voltages. These low values produce low currents in transistors $M_{n2,2}$ and $M_{n2,3}$. In this way, the output current and, consequently, the DC-level of V_o depends only of the transistors of the first cell. Now, by combining the currents in $M_{n1,1}$ and $M_{p1,1}$ is obtained

$$\beta_{M_{n1}} (V_{in1} - V_{THN})^2 = \beta_{M_{p1}} (V_{DD} - V_o - |V_{THP}|)^2 \quad (8)$$

where $\beta = 0.5k'W/L$ is the current factor. By associating the DC components of V_{in1} and V_o to V_{DC} , the expression (8) becomes

$$V_{DC} = \frac{V_{DD} - |V_{THP}| + \sqrt{\frac{\beta_{M_{n1}}}{\beta_{M_{p1}}} V_{THN}}}{1 + \sqrt{\frac{\beta_{M_{n1}}}{\beta_{M_{p1}}}}} \quad (9)$$

This is the same expression as the corresponding to the gate threshold voltage of a CMOS inverter. Now, considering the current in the transistor M_{off}

$$I_{b1} = \beta_{M_{off}} (V_{o1} - V_{DC} - V_{THN})^2 \quad (10)$$

and by substituting (9) in (10) it is obtained the DC component of the output

$$V_{o1} = V_{OD_{M_{off}}} + \frac{V_{DD} - |V_{THP}| + \sqrt{\frac{\beta_{M_{n1}}}{\beta_{M_{p1}}} V_{THN}}}{1 + \sqrt{\frac{\beta_{M_{n1}}}{\beta_{M_{p1}}}}} \quad (11)$$

where $V_{OD_{M_{off}}}$ is the overdrive voltage of M_{off} .

Design remarks:

1. Design transistors M_{p1} and M_{n1} with the aspect ratios required to obtain a CMOS inverter with threshold voltage $V_{DD}/2$.
2. Design transistor M_{n2} to obtain the same current of transistor M_{p1} (or a similar current).
3. The DC component of the output voltage can be shifted from $V_{DD}/2$ by a positive voltage given by

$$V_{OD_{M_{off}}} = \sqrt{\frac{I_{b1}}{\beta_{M_{off}}}} \quad (12)$$

4. For an N-input LTA circuit, the non-dominant pole will be given by $p_y = Ng_{m_{M2}}/(2\pi NC_y)$, therefore equation (7) is still valid if C_y is multiplied by N .

Fig. 4. Time domain simulation of the MIN circuit.

5. The presented approach has a complexity of $3N + 1$ transistors per N -input or $3N + 3$ if the DC level shifter is included.

5 Simulations and experimental results of the MIN circuit

The simulation of the LTA circuit of Fig. 3 was performed using HSpice and the parameters of a $0.5\ \mu\text{m}$ CMOS technology from ON-Semi foundry. The aspect ratio of transistors are the same detailed in Table I, with $V_{DD} = 1.5\ \text{V}$, $I_b = 90\ \mu\text{A}$, $C_L = 1\ \text{pF}$ and $C_c = 50\ \text{fF}$. The aspect ratios of the transistors were designed using the procedure presented in section 4, while the DC level shifter was designed to obtain input and output DC components of $1.1\ \text{V}$. It corresponded to $I_{b1} = 24\ \mu\text{A}$ and $W_{Moff}/L_{Moff} = 13.2\ \mu\text{m}/1.5\ \mu\text{m}$. Fig. 4 shows the time domain simulation of the LTA output when the inputs are two sinusoidal signals with frequencies of $2\ \text{MHz}$ and $1\ \text{MHz}$, respectively, and a triangular signal with frequency of $1\ \text{MHz}$. Peak to peak amplitudes of $0.5\ \text{V}$ were used in order to use the complete working range of the involved basic cells. For clarity, an inverted output has been depicted in this figure. This output presents the desired behavior, following the signal corresponding to the minimum value with a maximum corner error of $10\ \text{mV}/10\ \text{ns}$. A corresponding Monte Carlo simulation in time domain with $n=1000$ was realized to evaluate the effect of mismatch components (tolerances in threshold voltages and current factors) in the performance of the LTA circuit, it in agreement with the Pelgroms mismatch model [15]. It is depicted in Fig. 7(a) while the corresponding histogram of the offset contributions in V_{o1} is depicted in Fig. 7(b). The small standard deviation $\sigma = 1.4\ \text{mV}$ is consequence of the low impedance of all the nodes of the LTA circuit.

The microphotograph of the fabricated MIN circuit is shown in Fig. 6 (a). A measurement of the circuit with three input voltages is shown in Fig. 6 (b). The highest input frequency of the sinusoidal signal was $500\ \text{kHz}$, the MIN

Fig. 5. Monte Carlo simulation.

Fig. 6. Fabricated LTA prototype. (a) LTA circuit microphotograph. (b) Measured oscilloscope traces of the LTA circuit.

output was inverted using the oscilloscope internal function in order to show a proper operation. The estimated loading capacitance due to the oscilloscope probe and parasitic effects from the PCB were quite large, $\approx 20\text{ pF}$. A comparison with other LTA circuits reported in the literature is shown on Table II.

6 Conclusions

A CMOS MIN circuit for low voltage applications was proposed. The architecture is based on a new configuration of follower stage with low-output impedance, which is able to work with voltages as low as 1.5 V . The circuit was validated with simulations results as well as with experimental measurements of a fabricated prototype with CMOS ON Semi $0.5\text{ }\mu\text{m}$ technology. The voltage output swing of the proposed circuit unlike the FVF proposed in [13]

Table II. Comparison among low complexity LTA circuits.

MIN circuit	Transistor count (n inputs)	CMOS Tech.	Corner error	$V_{DD} - V_{SS}$
[7]	$7n + 1$	$0.25\ \mu m$	$25\ mV/100\ ns$	$3\ V$
[8]	$7n + 1$	$1.6\ \mu m$	$15\ mV/10\ ns$	$5\ V$
[9]	$5n + 3$	$0.25\ \mu m$	$10\ mV/5\ ns$	$2.5\ V$
[10]	$7n + 4$	(SOI) $3\ \mu m$	—	$1.5\ V$
[11]	$7n$	$0.8\ \mu m$	$40\ mV/10\ ns$	$5\ V$
[12]	$3n + 3$	$0.5\ \mu m$	$15\ mV/15\ ns$	$1.5\ V$
[13]	$5n$	$0.5\ \mu m$	$15\ mV/40\ ns$	$3\ V$
This work	$3n + 1$	$0.5\ \mu m$	$10\ mV/10\ ns$	$1.5\ V$

can be increased as a larger voltage supply is used. In agreement with Table II, the proposed LTA circuit can be considered of low-complexity ($3N+1$). The basic cell presents good electrical features (for instance $THD \approx 1\%$) and could be used for other analog applications.

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