Contact resistivity reduction for PtSi/Si(100) by dopant segregation process

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Abstract: Contact resistivity reduction at PtSi/Si(100) interface by dopant segregation (DS) process was investigated by the cross-bridge Kelvin resistor (CBKR) method for the first time. After the 60 nm-thick PtSi was formed at 700°C/1 min in N₂ ambient, ion implantation (PH₃ or BF₃, $1 \times 10^{15} \text{ cm}^{-2}$, 15 keV) was carried out followed by the drive-in anneal at 800°C/1 min as a DS process. The Schottky barrier height (SBH) for electron and hole obtained from the C-V characteristics of PtSi/Si(100) diodes were 0.19 eV and 0.23 eV, respectively. The contact resistivity of $1.7 \times 10^{-7} \Omega \text{ cm}^2$ for PtSi/p⁺-Si(100) and $1.8 \times 10^{-6} \Omega \text{ cm}^2$ for n⁺-Si(100) were achieved even for the minimum contact area of 2.2 μm^2 and 33 μm^2 , respectively.

Keywords: PtSi, dopant segregation, work function, contact resistivity

Classification: Electron devices, circuits, and systems

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1 Introduction

The contact resistance (R_c) at silicides and source/drain diffusion regions is necessary to be reduced for scaled MOSFETs [1]. PtSi shows excellent

thermal budget immunity up to 800°C and low Schottky barrier height (SBH) for hole (Φ_{bp}) which is suitable for the pMOSFETs, while its SBH for electron (Φ_{bn}) is relatively high (0.87 eV), which leads to a degradation of current drivability in nMOSFETs because of the high contact resistance compared to that of NiSi [2]. We have reported that the alloying with low work function metal, such as Hf (ϕ_m : 3.9 eV) to reduce Φ_{bn} of PtSi, and the Φ_{bn} of 0.53 eV and contact resistivity (ρ_c) of $2 \times 10^{-7} \Omega\text{cm}^2$ to n⁺-Si(100) at the contact area of $4 \mu\text{m}^2$ were achieved [3, 4, 5]. However, the barrier height should be reduced down to 0.2 eV for further reduction of ρ_c such as $10^{-9} \Omega\text{cm}^2$ or below.

In this paper, we investigated the dopant segregation (DS) process to reduce the ρ_c at PtSi/n-Si(100) interface [6], and evaluated the ρ_c by cross-bridge Kelvin resistor (CBKR) method [7] for the first time.

2 Experimental procedure

Figure 1 shows schematic cross-sections of PtSi/Si(100) Schottky diodes (Figs. 1 (a) and 1 (b)) and CBKR structures (Fig. 1 (c)) fabricated in this study. After the patterning of the contact holes ($100 \times 100 \mu\text{m}^2$) on SiO₂ (350 nm)/Si(100), 40 nm-thick Pt layer was deposited on the substrates at room temperature (RT) by RF magnetron sputtering method. The gas pressure in the chamber during deposition was 0.65 Pa (Ar: 4.2 sccm). Silicidation was performed by a rapid thermal annealing (RTA) system in a flowing N₂ ambient at 700°C for 1 min. The selective etching was carried out to remove unreacted Pt in a solution of HCl:HNO₃:H₂O at 35°C. Ion implantations of PH₃ or BF₃ ($1 \times 10^{15} \text{cm}^{-2}$, 15 keV) for PtSi formed on p- and n-Si(100), respectively, were carried out for DS process followed by the drive-in anneal at 600-800°C/1 min in N₂ ambient. Finally, Al layer was evaporated and patterned to form the Schottky barrier diodes.

Fig. 1. Schematics cross-sections of (a) PtSi/p⁺/n-Si(100), (b) PtSi/n⁺/p-Si(100) Schottky diodes, and (b) CBKR structures with a dopant segregation process.

For the evaluation of ρ_c at PtSi/Si(100) interface, CBKR structures were fabricated as shown in Fig. 1 (c) [3, 7]. The p- and n-Si(100) substrates with 350 nm-thick thermal oxide were used as a starting substrates for the CBKR structure fabrication. The n⁺ and p⁺ heavily doped regions were formed by PH₃ and BF₃ ion implantations ($5 \times 10^{15} \text{cm}^{-2}$, PH₃: 30 keV, BF₃: 20 keV), respectively, followed by the sputtering of 200 nm-thick SiO₂ and activation annealing of 1000°C for 1 min in N₂ ambient. Then, the contact hole patterning was carried out for silicidation. The contact size (L) was designed as 1.5–16 μm [3]. The PtSi

layers were formed in a same manner described above. DS process (PH_3 , $1 \times 10^{15} \text{ cm}^{-2}$, 15 keV) was carried out for PtSi/n⁺-Si structures. Finally, Al-pad layer was patterned in a solution of $\text{H}_3\text{PO}_4\text{:HNO}_3$. The fabricated CBKR structures were annealed in a forming gas ($\text{N}_2\text{:}4.9\%\text{H}_2$) ambient at 400°C for 20 min.

SBH was obtained from the C-V characteristics for fabricated PtSi/Si(100) Schottky diodes. The ρ_c of PtSi/Si(100) structures was extracted by the CBKR method. The cross-section of CBKR structures was observed by transmission electron microscopy (TEM).

3 Results and discussion

Figure 2 (a) shows the drive-in temperature dependence of $1/C^2$ -V plots for PtSi/Si(100) Schottky diode formed by DS process. The measurement frequency of C-V was 1 MHz. The linear dependences were clearly observed for the PtSi Schottky barrier diodes formed by DS process both on p- and n-Si(100) as shown in Fig. 2 (a). SBH (Φ_b) was extracted from the slope of $1/C^2$ -V plots utilizing equations (1) and (2).

$$\frac{1}{C^2} = \frac{2}{q\epsilon_s\epsilon_0 N_B} (\Phi_b - V) \quad (1)$$

$$\Phi_{bp} = E_g - \Phi_{bn} \quad (2)$$

where C is the capacitance, V is the applied voltage, q is the elementary charge, ϵ_s is the relative dielectric constant of Si, ϵ_0 is the dielectric constant in vacuum, N_B is the doping concentration of Si substrates (10^{15} cm^{-3}), and E_g is the bandgap of Si.

Fig. 2. Drive-in temperature dependence of (a) $1/C^2$ -V plots and (b) the extracted SBH of PtSi/Si(100) Schottky diodes formed by DS process.

Figure 2 (b) shows the drive-in temperature dependence of SBH for the Schottky barrier diodes fabricated by DS process. It was found that the Φ_{bn} was remarkably reduced by 600–800°C drive-in anneal from 0.38 eV (as-implantation) to 0.19 eV. Φ_{bp} reduction was also observed, and Φ_{bp} of 0.23 eV was obtained by 800°C drive-in anneal, while it was 0.3 eV in case of 700°C drive-in anneal. Therefore, drive-in anneal was carried out at 800°C

for the CBKR process.

Next, the ρ_c of PtSi to heavily doped Si was evaluated by CBKR method. Figure 3 shows the contact area ($S=L^2$) dependence of ρ_c at the interface of silicides to p^+ - (Fig. 3 (a)) and n^+ -Si(100) (Fig. 3 (b)). The standard four-terminal CBKR pattern was used to determine the ρ_c by one-dimensional (1D)-model analysis [3]. The DS process was carried out for PtSi/ n^+ -Si(100) structures. Figure 3 (a) shows the contact area dependence of ρ_c at the PtSi/ p^+ -Si(100) interface. The cross-sectional TEM image for the fabricated CBKR structure is shown as an inset in Fig. 3 (a). From the TEM image, uniform PtSi layer was observed, and the physical thickness of PtSi was confirmed as 60 nm. It was found that the ρ_c of PtSi/ p^+ -Si(100) structures decreased to $1.7 \times 10^{-7} \Omega\text{cm}^2$ at the minimum contact area of $2.2 \mu\text{m}^2$. Figure 3 (b) shows the contact area dependence of ρ_c for the PtSi/ n^+ -Si(100) structures with DS process. From the result of Fig. 3 (b), the ρ_c of $1.8 \times 10^{-6} \Omega\text{cm}^2$ ($S=33 \mu\text{m}^2$) was obtained for PtSi/ n^+ -Si(100) structure.

Fig. 3. Contact area dependence of ρ_c for fabricated CBKR structures. (a) Al/PtSi/ p^+ -Si(100), and (b) Al/PtSi/ n^+ -Si(100). The cross-sectional TEM image for fabricated CBKR structure is shown as the inset in Fig. 3 (a).

As shown in Fig. 3, the obtained characteristics still show the clear dependence on the contact area. These results suggested that the current crowding occurs in the contact region [8], which makes the effective contact area small. Therefore, the decrease of contact area, for example $0.01 \mu\text{m}^2$, would realize the lower ρ_c such as $4 \times 10^{-9} \Omega\text{cm}^2$ for p^+ -Si, and $1 \times 10^{-9} \Omega\text{cm}^2$ for n^+ -Si, as shown by the dotted lines in Figs. 3 (a) and 3 (b). The extracted ρ_c values are speculated theoretically from the obtained SBH of 0.19 eV for n^+ -Si and 0.23 eV for p^+ -Si shown in Fig. 2 (b).

4 Conclusions

The reduction of SBH of PtSi/Si(100) by DS process was investigated, and evaluated the ρ_c by CBKR method for the first time. The Φ_{bn} and Φ_{bp} obtained from the C-V characteristics of PtSi/Si(100) diodes with DS process were 0.19 eV and 0.23 eV, respectively. The results for extracted ρ_c of $1.7 \times 10^{-7} \Omega\text{cm}^2$ to p^+ -Si ($S=2.2 \mu\text{m}^2$) and $1.8 \times 10^{-6} \Omega\text{cm}^2$ to n^+ -Si

($S=33\ \mu\text{m}^2$) were achieved for PtSi/Si(100) with DS process especially for $\text{n}^+\text{-Si}(100)$. From the contact area dependence of ρ_c , the ρ_c of PtSi/Si(100) would be expected to decrease to $4 \times 10^{-9}\ \Omega\text{cm}^2$ for $\text{p}^+\text{-Si}$, and $1 \times 10^{-9}\ \Omega\text{cm}^2$ for $\text{n}^+\text{-Si}$, when the contact area is $0.01\ \mu\text{m}^2$.

Acknowledgments

The authors would like to thank Prof. Emeritus H. Ishiwara, Mr. D. Shoji, Mr. Y. Yoshimura, and Mr. A. Yoshimi of Tokyo Institute of Technology, Prof. T. Ohmi and Dr. H. Tanaka of Tohoku University for their support and useful discussions for this research. This work was partially supported by TANAKA HOLDINGS Co. Ltd.