A high-resolution stochastic time-to-digital converter with edge-interchange scheme

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Abstract: A high-resolution stochastic time-to-digital converter (STDC) using an edge-interchange scheme is described. The proposed STDC provides a higher resolution but consumes less power than previous STDCs that gave the same resolution. The limitation on input phase difference caused by the arbiter and the edge-interchange circuit is analyzed. Simulated results show that for the task proposed herein, a resolution of up to 0.3 ps is achieved while only 1.7 mW is consumed. Furthermore, higher resolution is achieved, more power will be reduced by using the edge-interchange circuit.

Keywords: stochastic TDC, high resolution, edge-interchange circuit

Classification: Integrated circuits

References

1 Introduction

High-resolution time-to-digital converters (TDCs) play an important role in various applications, such as digital phase-locked loops, high-energy physics experiments, and laser radar devices. The Vernier method [1] suffers from a mismatch in gate delays. Pipeline TDCs based on time amplifiers [2] have disadvantages of large area, complex design and sensitivity to process, voltage and temperature (PVT) variations. A stochastic TDC (STDC) [3] employs a set of identical arbiters that exhibit random mismatches following a Gaussian distribution. The mismatches have a ‘dithering’ effect on outputs, which is equivalent to adding a random time offset TOS to one input of each ideal arbiter, as shown in Fig. 1. This structure simultaneously exhibits good PVT immunity and high resolution, with the penalties of a higher power consumption and a larger area because the resolution is proportional to the number of arbiters used in an STDC.

In this paper, an improved STDC that uses an edge-interchange scheme is presented. The edge-interchange scheme, which achieves dynamic element matching [4], doubles the equivalent number of arbiters and thereby improves the resolution by a factor of two. We also discuss the limitation on the phase difference between input clocks, which is caused by the arbiter and the edge-interchange circuit.

![Fig. 1. Concept of an STDC](image)

2 Proposed STDC

Fig. 2 (a) shows the proposed STDC, which is composed of an edge-interchange circuit, an arbiter array, and an encoder. In the edge-interchange circuit, the signal SC is generated by the falling edge of START and passed to the encoder as a sampling clock. The rising edges of START and STOP are output through CLK1 and CLK2 commutatively, which resembles the operation of dynamic element matching, as shown in Fig. 2 (b). The arbiter array com-
prises 64 identical arbiters that detect which input signal is the first to arrive. To achieve dynamic element matching, the arbiter circuit should be implemented in a differential structure. An OR gate is employed to control the charging of M5 and M6, which prevents the falling edges of the inputs from changing output state. The encoder sums the outputs of the arbiters and converts the summation to binary code.

In an STDC, the time offset $T_{OS}$ of each arbiter approximates a Gaussian random variable with standard deviation $\sigma_T$. According to [3], the resolution of an STDC can be expressed as

$$t_R = \frac{\sqrt{2\pi} \sigma_T}{N}$$

where $N$ is the number of arbiters. The resolution is usually improved by using more arbiters at the cost of a higher power dissipation and a larger area [5]. The resolution can be doubled using the proposed edge-interchange scheme, rather than simply increasing the number of arbiters. The random offsets of the arbiters can be defined as an array $T$: \{ $T_{OS1}$, $T_{OS2}$, ..., $T_{OSN}$ \}. The standard deviation of $T$ is given by

$$\sigma_T = \frac{1}{\sqrt{N}} \sum_{i=1}^{N} T_{OSi}^2 - \bar{T}^2$$

where $\bar{T}$ is the expectation of $T$. Because the offsets approximately follow a standard normal distribution, $\bar{T}$ is close to zero. (2) can therefore be rewritten as

$$\sigma_T \approx \frac{1}{\sqrt{N}} \sum_{i=1}^{N} T_{OSi}^2$$

In the proposed STDC, the rising edges of the inputs are interchanged cyclically due to the presence of the edge-interchange scheme. Therefore, the offset of each arbiter exhibits opposite polarities between adjacent cycles of START. In a cycle of SC (i.e., two adjacent cycles of START), the encoder receives $2N$ outputs, which is similar to $2N$ equivalent arbiters in the array. Therefore, the offsets can be defined as $T'$: \{ $T_{OS1}$, $T_{OS2}$, ..., $T_{OSN}$, $-T_{OS1}$, $-T_{OS2}$, ..., $-T_{OSN}$ \}. The expectation of the array $T'$ vanishes identically due to its symmetry, and the standard deviation can be determined by

$$\sigma_{T'} = \frac{1}{\sqrt{2N}} \left( \sum_{i=1}^{N} T_{OSi}^2 + \sum_{i=1}^{N} (-T_{OSi})^2 \right) - \bar{T'}^2$$

$$= \frac{1}{\sqrt{N}} \sum_{i=1}^{N} T_{OSi}^2 \approx \sigma_T$$

where $\bar{T'}$ is the expectation value of $T'$. Thus the resolution of the proposed STDC is

$$t_R' = \frac{\sqrt{2\pi} \sigma_{T'}}{2N} \approx \frac{1}{2} t_R$$

From (5), it can be seen that the achievable resolution is improved by a factor of two due to the use of the proposed edge-interchange scheme.
Because the transfer function of an STDC approximates the Gaussian error function, the linear region is limited to $\pm \sigma_T$, which is also the effective input range. Comparing (4) with (2), the effective input range of the proposed STDC is at least as wide as that shown in previous work [3, 5]. It should be noted that the OR gate output $V_G$ exhibits only a slim strip of low-level voltage when the phase difference between START and STOP is approximately $\pi$ (e.g., the $k$th and $k+1$th cycle in Fig. 2(b)). This results in M5 and M6 having insufficient time to charge their drain terminals prior to the next detection. Therefore, a certain margin is required to guarantee the proper functioning of the arbiter circuit. However, this limitation mostly has no effect for input frequencies lower than 16 GHz, because the time interval should remain within the linear region and is generally less than 20 ps.

![Image](image_url)

Fig. 2. (a) Structure, and (b) Timing diagram of the proposed STDC

3 Simulation results

To verify the performance of the proposed STDC, we simulated it using 0.13\,\mu m CMOS technology with a supply of 1.2 V and a clock frequency of 40 MHz. The edge-interchange circuit and encoder consume 0.3 mW and
Fig. 3. (a) Power reduction and resolution versus arbiters used, (b) Characteristic of the proposed STDC, and (c) DNL and INL of the proposed STDC
Table I. Performance comparison

<table>
<thead>
<tr>
<th></th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.35µm</td>
<td>0.09µm</td>
<td>0.13µm</td>
<td>0.13µm</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>&gt;5MHz</td>
<td>10MHz</td>
<td>75MHz</td>
<td>40MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>22.7ps</td>
<td>1.25ps</td>
<td>0.7ps</td>
<td>0.3ps</td>
</tr>
<tr>
<td>Power</td>
<td>2.7mW</td>
<td>3.6mW</td>
<td>2.7mW</td>
<td>1.7mW</td>
</tr>
<tr>
<td>Maximum nonlinearity</td>
<td>0.9LSB</td>
<td>3LSBs</td>
<td>2LSBs</td>
<td>2.5LSBs</td>
</tr>
</tbody>
</table>

0.1 mW respectively while the 64-unit-array consumes 1.28 mW, which means the proposed STDC saves power by 36.8% comparing with the conventional STDCs [3, 5] that achieve the same resolution. Such an advantage will become greater when more arbiters are used to pursue higher resolution. As shown in Fig. 3 (a), the power reduction reaches to 49.16% while 1,024 arbiters are used to achieve a high resolution up to 18.4 fs. Figs. 3 (b) and 3 (c) show the relationship between the time interval and the output code, and the linearity performance in the effective region, respectively. Two inputs with 0.05 Hz difference in frequency at 40 MHz are applied to generate a ramp input. DNL and INL are calculated from code density analysis with over one million hits. The linearity deteriorates in the region beyond the effective range (σT equals 15 ps in this design). Table I summarizes the performance comparison between our design and other works [1, 2, 3].

4 Conclusion

We have herein proposed an improved STDC that uses an edge-interchange technique that simultaneously provides high resolution and requires low power. We have also discussed the limitation on input phase difference caused by the arbiter and the edge-interchange circuit. Simulation results indicate that the realized resolution is 0.3 ps and the nonlinearity in the effective region is about 2.5 LSBs. The total power is only 1.7 mW thanks to the use of the edge-interchange scheme.

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