Data and edge decision feedback equalizer with > 1.0-UI timing margin for both data and edge samples

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Abstract: A 3-Gbps decision feedback equalizer (DFE) compensating for data and edge inter-symbol interference (ISI) is presented. A speculative architecture is employed to relieve the timing burden on the feedback signal for the DFE wherein the ISI of edge sample is compensated by speculating the DFE based on two-UI earlier data sample. Thereby, the timing margins of the DFE for data and edge ISI compensation are ensured to be larger than 1.0-UI. The proposed DFE has been implemented in a 0.13-µm CMOS technology together with a clock and data recovery (CDR) circuit. The DFE and CDR circuits occupy 0.28-mm² active area and the DFE consumes 18-mW from a 1.2-V supply. The RMS jitter of the recovered clock is improved from 15.6-ps to 11.9-ps by the proposed edge ISI compensating DFE.

Keywords: DFE (decision feedback equalizer), speculative DFE, inter-symbol interference (ISI), clock and data recovery (CDR), CMOS

Classification: Integrated circuits

References
1 Introduction

In order to avoid any erroneous clock and data recovery (CDR) in high-speed serial link, the inter-symbol interference (ISI) has to be reduced as much as possible before the sampling of the serial data input [1]. Although continuous-time linear equalizer (CTLE) is a well-known and widely adapted technique for the compensation of ISI, it amplifies the unwanted high-frequency noise as well [2]. A decision feedback equalizer (DFE) can cancel the post-cursor ISI without any high-frequency noise enhancement [3]. In a DFE, the results of the decision of previously received symbols have to be fed back to the current symbol before it is decided whether the current symbol is “1” or “0” [4]. Therefore the delay of the feedback loop has to be smaller than 1-UI to compensate the ISI at the center of the data eye, that is, the data sample [5]. The amount of the ISI at the edge of the data eye may be different from that of the ISI at the center of the data eye. Because a bang-bang phase detector (PD) based CDR recovers clock from the phase of the edge of the data eye, that is, edge sample, the ISI at the edge of the data eye has to be carefully compensated [6]. The delay of the feedback loop compensating the ISI of edge sample has to be smaller than 0.5-UI, which is a very stringent requirement.

There have been several techniques proposed to solve the above mentioned stringent requirements on the feedback path delay. A speculative DFE may relieve the timing burden of the feedback path compensating the ISI of data sample [7, 8]. If the ISI of edge sample is to be compensated independently, however, the feedback path has to be settled in less than 0.5-UI even with the speculative architecture. The first post-cursor ISI may be cancelled by feedforward equalization and thereby the timing burden is greatly reduced [9]. The feedforward path, however, was realized by a sample-and-hold (S/H) circuit which may generate feedthrough noise. In [10], either zero-offset edge sample or non-zero-offset edge sample is selected as the input of the CDR loop filter based on three consecutive data samples to avoid the bi-modal jitter distribution of the CDR output. Because the current data sample has to be determined before selecting the edge sample, however, the timing margin cannot be relaxed.

In this paper, a 3-Gbps DFE capable of compensating for the data and edge ISI with larger than 1-UI timing margin for the feedback path is presented. A CTLE preceding the DFE reduces long-tail ISI and a following one-tap speculative DFE cancels the first post-cursor ISI without amplifying high frequency noise. The stringent timing requirement on the feedback path
for edge ISI compensation has been relieved by controlling the speculative edge DFE with two-UI earlier symbol. In section II, the operation principle of the proposed data and edge DFE is explained and the circuit implementation is also described. The experimental results are shown in section III and finally the conclusion is given in section IV.

2 Data and edge decision feedback equalizer with relaxed timing requirements

Fig. 1 shows the architecture of a high-speed serial link receiver employing the proposed data and edge DFE and bang-bang PD based CDR circuit. A one-stage boosting amplifier is used as a CTLE to ensure the sufficient data eye opening for the DFE to work properly. The voltage controlled oscillator (VCO) generates 16-phase clocks among which $CLK_I(0:7)$ and $CLK_Q(0:7)$ are used for the sampling of edge and data of serial input, respectively. The phase of the VCO output clocks is controlled to track that of the serial data input by the CDR loop comprising the transition detector, charge pump (CP) and loop filter (LF). The samplers of the DFE are used as PD for the CDR operation. Based on the sampler outputs of the DFE, the transition detector generates $UP$ and $DN$ signals to move the phase of the VCO towards the desired point. The frequency of the VCO in the CDR loop is coarsely controlled by the phase locked loop (PLL) which employs the same VCO as the one in the CDR loop.

2.1 Compensation of edge ISI with > 1-UI timing margin

If we consider two previous symbols and current symbol together, there are

Fig. 1. Receiver architecture with the proposed data and edge decision feedback equalizer (DFE).
eight possible data patterns. Among them, “100”, “011”, “111”, and “000” do not have any transition edge for the current symbol and there is no information useful for the CDR. Therefore, for the compensation of edge ISI, it is sufficient to consider only the patterns “101”, “110”, “010”, and “001”. For these input data patterns, the ISI effects are shown in Fig. 2. For the patterns “101” and “010”, the transition edge becomes earlier than that for the case without ISI while for the patterns “110” and “001”, the transition edge gets later. To move the transition edge towards the ideal position, the voltage level of the positive (negative) input at the edge of the current symbol $DQ_{h,n}$ has to be pulled up (down) by certain amount for the data patterns “010” and “001”. On the other hand, the voltage level of the positive (negative) input at the edge of the current symbol has to be pulled down (up) for the data patterns “101” and “110”. In summary, the voltage level of the positive (negative) input at the edge of the current symbol $DQ(n)$ has to be pulled up (down) when $DQ(n-2)$ is “0” and “1”, respectively to move the transition edge of the current symbol towards the ideal position. This means the edge ISI of $DQ(n)$ can be compensated based on the decided symbol of $DQ(n-2)$. Therefore, the feedback path of the DFE for the compensation of the edge ISI is allowed to have 1.5-UI delay.

Fig. 3 shows the simulated waveforms of 3-Gbps serial data at the end of a cable with 10-dB loss at 1.5-GHz for the patterns “0101”, “1101”, “0001”, and “1001”. The transition edge of $DQ(n)$ for the data pattern “0001” (“1001”) lags that for the data pattern “1101” (“0101”) although $DQ(n-1)$ is “0” (“1”) for both the data patterns. This is because $DQ(n-2)$ is different. From this observation, it is apparent that a conventional one-tap DFE is insufficient to compensate the edge ISI and more than two taps are required. On the contrary, the proposed edge ISI compensation technique provides similar performance as two-tap DFE with only one tap because $DQ(n-2)$ is used to compensate the edge ISI.
2.2 Implementation

Fig. 4 shows the architecture of the proposed one-tap DFE with independent data and edge ISI compensation. The ISI of the data and edge samples is compensated by separate circuits, that is, $EDGE\_CELL(i)$ and $DATA\_CELL(i)$, respectively. The operation timing of the proposed DFE circuit is shown in Fig. 5. The proposed DFE has the speculative architecture to relieve the timing requirements on the feedback path. For the ISI compensation of data sample $DATA(i)$, one-UI earlier sample $DATA(i - 1)$ is used to select one between the two speculative outputs $D_P(i)$ and $D_N(i)$. For edge
sample $EDGE(i)$, $DATA(i-2)$ is used to select one between the two speculative outputs $EP(i)$ and $EN(i)$.

The outputs $EDGE(0:7)$ and $DATA(0:7)$ of the data and edge samplers are combined to detect the transition of the input data and generate $UP$ and $DN$ signals for the phase tracking of the CDR.

### 3 Experimental results

The proposed data and edge DFE has been implemented in a 0.13-µm CMOS technology. Its chip microphotograph and detailed layout are shown in Fig. 6. The active area is 0.28-mm$^2$ including the CDR circuitry. The proposed DFE consumes 18-mW from a 1.2-V supply.

All the measurements have been performed with $2^{31}-1$ pseudo-random binary sequence (PRBS) input and the loss of the cable is 20-dB at 1.5-GHz. Fig. 7-(a) shows the eye diagram at the input of the receiver and the CTLE preceding the DFE improves the eye for the DFE and CDR to operate...
Fig. 7.  Eye diagram of (a) the receiver input (b) and DFE input for 3-Gbps $2^{31}-1$ PRBS input with 20-dB cable loss.

Fig. 8.  Jitter of the CDR output clock (a) without and (b) with the edge ISI compensation by the proposed DFE.
properly as shown in Fig. 7-(b). The jitter of the CDR output clock is shown in Fig. 8-(a) and -(b) without and with the proposed DFE. With the proposed DFE, the jitter is improved from 15.6-ps,rms to 11.9-ps,rms because the deterministic jitter at the edge samples can be minimized.

The bit error rate (BER) bathtub curve of the recovered data is shown in Fig. 9. With the proposed DFE, the eye opening for the BER of $10^{-12}$ is improved from 0.46-UI to 0.67-UI. Fig. 10 shows the tolerance of the CDR to the sinusoidal jitter for BER smaller than $10^{-12}$. The CDR tracking bandwidth is about 1-MHz and the high-frequency jitter tolerance is 0.3-UIpp.

The performance of the proposed DFE is summarized in Table I. Without any cable loss, the eye opening for the BER of $10^{-12}$ is 0.79-UI which is

![Fig. 9. BER bathtub curve of the recovered data (a) without and (b) with the edge ISI compensation by the proposed DFE.](image)

![Fig. 10. Measured sinusoidal jitter tolerance of the CDR for BER $< 10^{-12}$.](image)

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<thead>
<tr>
<th>Items</th>
<th>without cable loss</th>
<th>with 20-dB cable loss</th>
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<tbody>
<tr>
<td>CDR clock jitter with RMS</td>
<td>6.83-ps</td>
<td>15.6-ps</td>
</tr>
<tr>
<td>$2^{31}$-PRBS input Peak-to-peak</td>
<td>70.4-ps</td>
<td>118-ps</td>
</tr>
<tr>
<td>Eye opening for $10^{-12}$ BER</td>
<td>0.79-UI</td>
<td>0.46-UI</td>
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reduced to 0.46-UI if there is 20-dB cable loss. By applying the proposed DFE, the opening is improved to 0.67-UI which is 85-% of the original eye opening without any cable loss.

4 Conclusions

A 3-Gbps DFE capable of compensating for the edge and data ISI independently with each other is presented. The timing margin for the feedback path of the speculative DFE is ensured to be larger than 1.0-UI for both the data and edge ISI compensation. A CTLE preceding the DFE reduces long-tail ISI and the following one-tap speculative DFE cancels the first post-cursor ISI without amplifying high-frequency noise.

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