Complementary 5T-4MTJ nonvolatile TCAM cell circuit with phase-selective parallel writing scheme

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Abstract: Towards a compact and process-variation-tolerant nonvolatile ternary content-addressable memory (TCAM), we propose a novel complementary cell structure with just five transistors and four magnetic tunnel junction (MTJ) devices (5T-4MTJ). The complementary cell structure enlarges output voltage swing of each cell circuit together with match-line voltage swing in word circuit constructed by many bits of cell circuits, which eliminates search errors. We also propose a novel bit-parallel writing scheme, called phase-selective parallel writing, for the cell circuit. Every data is written into a complementary MTJ-device pair in two phases by selectively asserting bit-lines during 0-write phase or 1-write phase, not directly assigning write data to the bit-lines. Consequently, the phase-selective parallel writing scheme enables four-phase write for the proposed 5T-4MTJ-based word circuit.

Keywords: spintronics, STT, complementary, bit-parallel, process variation, associative memory

Classification: Integrated circuits

References

1 Introduction

Ternary content-addressable memories (TCAMs) are attractive information retrieval hardware with highly parallel processing capability for a number of applications [1, 2]. Conventional static random access memory (SRAM)-based TCAMs tend to suffer from an area penalty, because bit-level comparison logic as well as two-bit storage functions must be implemented in a single cell circuit. Moreover, standby power dissipation due to leakage current in the SRAM-based TCAM is increasingly dominating in recent nanometer-scale CMOS era. In addition, process variation is also a significant problem in the nanometer-scale integration. Since some kinds of SRAM cell circuits with more transistors have been reported for immunity from the process variation, SRAM-based TCAMs may encounter the same situation.

In order to realize compact and standby-power-free bit-parallel TCAMs, we have proposed magnetic tunnel junction (MTJ)-based nonvolatile TCAMs using several kinds of cell circuits such as nine-transistor/two-MTJ-device (9T-2MTJ), 7T-2MTJ, 6T-2MTJ and 4T-2MTJ [2, 3, 4, 5, 6]. Since the 9T-2MTJ and 7T-2MTJ cell circuits include sense amplifiers, full-voltage outputs are generated from the cell circuits, which easily realizes bit-parallel search operation with many bits of cells in a word circuit. On the other hand, since output voltage swings of the 6T-2MTJ and 4T-2MTJ-based cell circuits are limited, output voltage swings of the word circuits (match-line voltage swings) are also limited. The limited output voltage swings of cell circuits and word circuits consisting of many bits are significant problems under process variation in nanometer-scale technology. Hence, it is required to increase output voltage swings of the limited voltage-swing cell circuits such as the 6T-2MTJ and 4T-2MTJ-based ones for bit-parallel search operations.

In this paper, we propose a novel complementary cell structure with just five transistors and four MTJ devices for bit-parallel search operation under serious process variation. We also propose a novel bit-parallel writing scheme, called phase-selective parallel writing, for fast write operations in the proposed nonvolatile TCAM.

2 Complementary 5T-4MTJ nonvolatile TCAM cell circuit with phase-selective parallel writing scheme

In this section, we briefly overview a conventional bit-parallel nonvolatile TCAM with a conventional 6T-2MTJ cell circuit. Then, we introduce a proposed 5T-4MTJ cell circuit with bit-parallel writing scheme for a process-variation-tolerant nonvolatile TCAM.
A fully-parallel TCAM is one of the most major TCAMs. It performs high-speed search operation, while it consumes high power because all the cells are simultaneously activated during the search operation. Word segmentation scheme shown in Fig. 1 is often utilized to reduce power consumption during the search operation. In this architecture, word circuits are segmented by sense amplifiers, and a search operation is completed in a single cycle by simultaneously assigning all the input bits to the cell array. Combination of

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**Fig. 1.** Low-power nonvolatile TCAM with segmented word structure.

**Fig. 2.** Nonvolatile TCAM cell circuits and their output voltage swings: (a) conventional 6T-2MTJ cell circuit, (b) output voltage swing of the 6T-2MTJ cell circuit, (c) proposed complementary 5T-4MTJ cell circuit, (d) output voltage swing of the 5T-4MTJ cell circuit.
the segmented architecture and power gating is especially suitable for non-volatile TCAMs. Latter segments consisting of more bits of cells are activated only when the prior segments consisting of smaller bits of cells are matched, which results in low active and standby power consumptions with power gating technique.

In order to realize such a segmented bit-parallel nonvolatile TCAM, cell circuit must be operated in parallel with many bits. We have utilized a 6T-2MTJ-based cell circuit shown in Fig. 2(a) for the bit-parallel nonvolatile TCAM. In this cell circuit, output voltage in HIT/MISS case is determined by the cross point between a current curve $I_{\text{HIT}} = I_{\text{MISS}}$ and a load current curve $I_{\text{LOAD}}$ as shown in Fig. 2(b). Output voltage swing of the cell circuit, $\Delta V_{CO}$, decreases along with variation of the currents flowing the cell circuit due to threshold-voltage variation of each transistor and resistance variation of each cell.

Fig. 3. Nonvolatile TCAM cell layouts: (a) conventional 6T-2MTJ twin-cell, (b) proposed complementary 5T-4MTJ cell.
MTJ device. One of the cell output voltages, $V_{CO-H}$ or $V_{CO-M}$, is conducted to match-line (ML). ML of each word circuit is initially charged to $V_{DD}$ in precharge phase for a search operation. When a stored word matches to an input key word (HIT), the ML is discharged to $V_{CO-H}$ in evaluation phase. When the stored word mismatches to the input key word (MISS), the ML is discharged to $V_{CO-M}$. Output of the word circuit is generated by sensing the ML-voltage swing using a sense amplifier, hence it should be large. Fig. 2(c) shows a proposed nonvolatile TCAM cell circuit with 5T-4MTJ. Because of the complementary cell structure, output voltage in HIT/MISS case is determined by the cross point between a current curve $I_{HIT} = I_{MISS}$ and its complementary load current curve $I_{0HIT} = I_{0MISS}$ as shown in Fig. 2(d), which enlarges $\Delta V_{CO}$ and ML-voltage swing compared to the conventional 6T-2MTJ cell circuit. In order to compactly realize the complementary cell circuit, cell transistors and cell wires except diode-connected transistor $M3$ and ML are completely shared. Vertical lines are used as bit-lines ($BL1/BL2$) in write mode, and search-lines ($SL/SL$) in search mode. Horizontal lines are used as plate-lines ($PL1/PL2$) in write mode, and power/ground-lines ($V_{DD}/GND$) in search mode. Two PL drivers are used to generate voltage signals of $PL1$ and $PL2$, or $V_{DD}$ and $GND$. As a result, the proposed cell shown in Fig. 3(b) can be compactly realized with area reduction of 30% compared to the conventional 6T-2MTJ cell shown in Fig. 3(a).

Fig. 4 shows simulated waveforms of bit-parallel writing scheme, called phase-selective parallel writing, together with search operations. During write mode, complementary pulse are supplied to $PL1$ and $PL2$ by PL drivers. Durations of $(PL1, PL2) = (0, 1)$ and $(PL1, PL2) = (1, 0)$ are called as 0-write phase and 1-write phase, respectively. Every data is written into a comple-
mentary MTJ-device pair in two phases by selectively asserting bit-lines during 0-write phase or 1-write phase, not directly assigning write data to the bit-lines. In case of the simulated waveforms, “0” and “1” are written into MTJ1 and MTJ1’, respectively. In the same way, “1” and “0” are written into MTJ2 and MTJ2’, respectively. In order to successfully write data into the proposed cell circuit, boosted voltages for PL1/PL2/BL1/BL2 and/or lower write current of MTJ device with lower resistance are required. The proposed phase-selective parallel writing scheme enables four-phase write for the proposed 5T-4MTJ-based word circuit, while the conventional 6T-2MTJ-based word circuit enables two-phase write. Therefore, the proposed phase-selective parallel writing scheme has twice write-cycle penalty.

3 Evaluation

In this section, we demonstrate evaluation results of sensing margins and error rates for search operations in conventional and proposed nonvolatile TCAMs.

We designed 72-bit nonvolatile TCAM word circuits using conventional 6T-2MTJ cell circuit and proposed 5T-4MTJ one. We evaluated worst-case sensing margins and error rates of the word circuits between “HIT” and 1-bit “MISS” by a 1000-run Monte Carlo simulation under 90-nm CMOS technol-
ogy. We used the same sense amplifier reported in [7]. $V_{DD}$ is set to 1.2 V. Clock cycle is set to 5 ns (200 MHz). We assumed random variations of all the transistors and MTJ devices in the designed word circuit. $\sigma$ of threshold voltage of each transistor is set based on its gate area and Pelgrom coefficient provided by the 90-nm CMOS technology. Resistance value of MTJ device in “0” state and “1” state are set to 3.0 k$\Omega$ and 7.5 k$\Omega$, respectively. $\sigma$ of each resistance is set to 5% of its typical value.

Fig. 5(a) shows simulated waveforms of 72-bit parallel search operation in conventional 6T-2MTJ-based word circuits. Because of small sensing margin of 39 mV, there are 1 error and 4 errors during detecting “HIT” and “MISS”, respectively, which results in error rate of 0.25% (=5/2000). The errors are removed in the proposed 5T-4MTJ-based word circuits with enlarged sensing margin of 204 mV by complementary cell structure as shown in Fig. 5(b). Because of the 5.2 times of sufficient ML-voltage swing, match delay during evaluation phase is reduced from 2.1 ns to 1.3 ns compared to the conventional word circuit.

4 Conclusion

We have proposed a complementary 5T-4MTJ cell circuit for a compact and process-variation-tolerant nonvolatile TCAM. The complementary cell structure enlarges output voltage swing of each cell circuit together with match-line voltage swing in word circuit, which results in no error in search operations with 5.2 times of sensing margin. Moreover, we have also proposed phase-selective parallel writing scheme resulting in four-phase write for the proposed 5T-4MTJ-based word circuit.

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