A 1.5–5.0 Gb/s clock and data recovery circuit with dual-PFD phase-rotating phase locked loop

Dong-Ho Choi and Changsik Yoo^{a)}

*Department of Electronics & Computer Engineering, Hanyang University,
222, Wangsimni-ro, Seoungdong-gu, Seoul, 131–791, Korea*

a) csyoo@hanyang.ac.kr

Abstract: A clock and data recovery (CDR) circuit for 1.5–5.0 Gb/s wireline transceiver is described. A phase locked loop (PLL) with dual phase frequency detector (PFD) and charge pump (CP) pairs performs the seamless phase rotation for the CDR circuit to track the phase and frequency difference. The CDR circuit implemented in a 65 nm CMOS process consumes 22.8 mW from a 1.2 V supply at 5.0 Gb/s. For 25 MHz jitter frequency, the CDR circuit can tolerate up to 0.21 unit-interval (UI) jitter with bit error rate (BER) smaller than 10^{-12} .

Keywords: clock and data recovery (CDR), wireline transceiver, phase locked loop (PLL), phase rotation, CMOS

Classification: Integrated circuits

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1 Introduction

High-speed serial link has been applied extensively to large bandwidth wireline data transmission systems due to its lower system implementation cost than that with a parallel link based system [1]. For the same system bandwidth, of course the per-lane data rate of a serial link based system has to be higher than that of a parallel-link based system. However, as the data rate of serial link increases, the timing margin gets smaller and the signal quality is also degraded due to higher channel loss [2]. The degraded signal integrity and smaller timing margin make the design of clock and data recovery (CDR) circuit ever challenging for higher data rate. Because the smaller timing margin at higher data rate is an unavoidable challenge, it has to be overcome by providing a low jitter clock and minimizing deterministic timing error such as duty cycle distortion and phase mismatch if multi-phase clocking is employed [3, 4, 5, 6].

There can be many ways of CDR depending on the clocking scheme of wireline data transmission system [7]. If a transmitter sends clock signal together with serial data to a receiver like in High-Definition Multimedia Interface (HDMI), the role of CDR circuit is relatively simple because it does not need to track the frequency offset between the transmitter and the receiver [8]. If no clock is forwarded from a transmitter to a receiver like in PCI-Express (PCI-E), Serial-ATA (SATA), and Universal Serial Bus (USB), however, there can be non-zero frequency difference between the transmitter and the receiver clocks. Then the CDR circuit has to be capable of tracking the phase and frequency difference between the transmitter and receiver [9]. For seamless phase rotation, analog phase interpolator is most widely used but its design is very complicated because the accuracy of the phase interpolation is heavily dependent on the slope of the input clock signals [10]. In [11], a phase

Fig. 1. Architecture of the wireline transceiver.

Fig. 2. Clock and data recovery circuit with phase rotating PLL.

locked loop (PLL) with dual phase frequency detector (PFD) and charge pump (CP) pair performs the seamless phase rotation for the CDR circuit to track the phase and frequency. The dual-PFD phase rotating PLL, however, has a false locking problem which will be explained in Section 2 in more detail. In [12], an enable signal is used to start the phase rotating operation at proper timing ensuring no false locking. The enable signal, however, has to be very carefully generated according to the desired output clock phase and the feedback clocks for the dual-PFD are fixed to be 0° and 180° ones. Conventionally, the feedback clocks have smaller spacing, for example 45° or 90°. If the spacing between the feedback clocks is large, the resolution of the phase rotation becomes worse.

In this paper, a CDR circuit for 1.5–5.0 Gb/s wireline transceiver is described which is targeted for PCI-Express Gen. 1/2 and Serial-ATA Gen. 1/2. A dual-PFD PLL performs the seamless phase rotation for the CDR circuit to track the phase and frequency difference between the transmitter and the receiver [11]. The false locking problem of the dual-PFD PLL is avoided by a newly proposed enabling scheme. Section 2 describes the architecture and circuit implementation of the CDR circuit and its measurement results are given in Section 3. Finally Section 4 concludes this paper.

Fig. 3. (a) Clock phase defined by the multi-phase clock outputs of the VCO and (b) the feedback clock selection code $PHSEL\langle 0:2 \rangle$ and the CP current ratio control code $CPWT\langle 0:5 \rangle$ that are required for the phase rotating PLL to position the input clock Φ_{IN} at a specific phase.

2 Clock and data recovery with phase rotating PLL

2.1 Transceiver architecture

Fig. 1 shows the architecture of the single-lane wireline transceiver of this work which consists of main PLL, receiver, and transmitter. This can be easily extended to multiple-lane wireline transceiver by placing the required number of receivers and transmitters while the main PLL is shared among the multiple receivers and transmitters.

From the reference clock input Φ_{REF} , the main PLL generates the multi-phase clock $\Phi_{CLK}\langle 0:3 \rangle$ for the CDR operation of the receiver and the parallel-to-serial conversion of the transmitter. The inter-symbol interference (ISI) of the differential inputs RxP and RxN is compensated by the linear equalizer to ensure the sufficient eye opening for the CDR circuit to be capable of extracting the phase information of the incoming data. The output of the linear equalizer is applied to the CDR circuit which determines the optimum sampling point of the serial data input. The recovered serial data output of the CDR circuit is then de-serialized to the 20-bit parallel output $RDQ\langle 0:19 \rangle$. In the transmitter, the 20-bit parallel input $TDQ\langle 0:19 \rangle$ is serialized with the multi-phase clock $\Phi_{CLK}\langle 0:3 \rangle$ provided by the main PLL. The serialized data is then driven to the differential data outputs TxP and TxN by a voltage mode driver for low power consumption [13].

Fig. 4. Timing diagram when $\Phi_{VCO<0>}$ and $\Phi_{VCO<1>}$ are selected as Φ_I and Φ_Q , respectively and the ratio $I_{CP_I} : I_{CP_Q}$ of the pumping currents of the two charge pumps CP_I and CP_Q is 2 : 1. The phase rotating PLL is (a) correctly locked with the phase of the input clock Φ_{IN} being $\pi/12$ and (b) falsely locked with the phase of the input clock Φ_{IN} being $17\pi/12$.

2.2 Clock and data recovery (CDR) with phase rotating PLL

In order for the CDR circuit to track the phase of the incoming serial data input, the phase of the sampling clock has to be capable of rotating 2π seamlessly. The CDR circuit of this work is based on a phase rotating PLL with dual-PFD/CP pairs which provides the seamless phase rotation without any stringent requirement on the slope of clocks which is critical for conventional analog phase interpolator [10]. As illustrated in Fig. 2, there are two feedback loops in the CDR circuit, that is, the phase rotating PLL and the CDR loop. The phase rotating PLL has dual-PFD/CP pairs with the output clock Φ_{IN} from the main PLL as the reference clock input.

At the locked state of the phase rotating PLL, the phase of the VCO is determined by the selected two adjacent feedback clocks— Φ_I and Φ_Q —and the ratio of the pumping currents of the two CPs (CP_I and CP_Q). The CDR

Fig. 5. (a) Detailed schematic of the PFD_Q and PFD_I preventing the false locking of the phase rotating PLL and (b) the timing diagram illustrating the enabling of the CDR operation and PFD_Q.

loop controls the ratio of the pumping currents of the two CPs and selects two adjacent clocks Φ_I and Φ_Q among the multi-phase VCO output clocks $\Phi_{VCO<0:7>}$. The CP current ratio control code $CPWT<0:5>$ and the feedback clock selection code $PHSEL<0:2>$ are generated by the digital loop filter (DLF) from the sampler outputs $DATA<0:3>$ and $EDGE<0:3>$ among which $DATA<0:3>$ is de-serialized to the 20-bit parallel output $RDQ<0:19>$.

Let's define the phase of the clocks with the multi-phase VCO clocks $\Phi_{VCO<0:7>}$ as shown in Fig. 3-(a). If the sampling clocks of the CDR circuit have the optimum phase when the phase of the input clock Φ_{IN} of the phase rotating PLL is $\pi/12$, the input clock Φ_{IN} has to be in the region $R0$ and the DLF should select the two adjacent clocks $\Phi_{VCO<0>}$ and $\Phi_{VCO<1>}$ as the feedback clocks Φ_I and Φ_Q , respectively by setting $PHSEL<0:2> = 000$ as shown in Fig. 3-(b). The pumping current ratio of the charge pumps CP_I and CP_Q is determined by the CP current ratio control code $CPWT<0:5>$ whose decimal equivalent value $CPWT_{EQ}$ ranges from 0 to 63. Let's define α as $CPWT_{EQ}/63$, then the pumping current I_{CP_I} of the charge pump CP_I is

$\alpha \cdot I_{CP}$ and the pumping current I_{CP-Q} of the charge pump CP_Q is $(1 - \alpha) \cdot I_{CP}$. If α is $1/3$, the phase rotating PLL would be locked when the phase of the input clock Φ_{IN} is $\pi/12$ because the net charge $(= T_{ERR-I} \times I_{CP-I} - T_{ERR-Q} \times I_{CP-Q})$ pumped to the loop filter is zero as shown in Fig. 4-(a).

In the region $R0$, $CPWT\langle 0:5 \rangle$ and therefore α has to be decreased to rotate the phase of the input clock Φ_{IN} counterclockwise. If α reaches zero but Φ_{IN} has to rotate further counterclockwise, the DLF has to set $PHSEL\langle 0:2 \rangle = 001$ to move to the region $R1$. In the region $R1$, $CPWT\langle 0:5 \rangle$ and therefore α has to be increased to rotate the phase of the input clock Φ_{IN} counterclockwise. In this manner, the clock phase can be rotated over 2π seamlessly.

2.3 False locking prevention of phase rotating PLL

For the correct operation of the CDR circuit, a special care has to be taken to avoid the false locking of the phase rotating dual-PFD PLL [12]. Fig. 4-(b) illustrates an exemplar false locking phenomenon when the same clocks $\Phi_{VCO}\langle 0 \rangle$ and $\Phi_{VCO}\langle 1 \rangle$ are selected and the current ratio is also same as the case shown in Fig. 4-(a). Because the phase difference between $\Phi_I = \Phi_{VCO}\langle 0 \rangle$ and Φ_{IN} is $7\pi/12$ and the phase difference between $\Phi_Q = \Phi_{VCO}\langle 1 \rangle$ and Φ_{IN} is $14\pi/12$, the net charge pumped to the loop filter is also zero and the PLL may be locked. The phase rotating PLL is falsely locked with the phase of the input clock Φ_{IN} being $17\pi/12$ while it has to be $\pi/12$ as shown in Fig. 4-(a).

Because the CDR loop is digitally controlled, there must be bang-bang jitter when the phase rotating PLL is locked. In Fig. 4-(a) and -(b), the rising edges of Φ_I and Φ_Q used for the phase comparison with Φ_{IN} are denoted as arrows. For the correct locking case in Fig. 4-(a), they are spaced by $\pi/4$ which is $7\pi/4$ for the false locking case in Fig. 4-(b). Therefore, compared to the correct locking case in Fig. 4-(a), the bang-bang jitter would be seven times larger when the PLL is falsely locked as shown in Fig. 4-(b) and therefore the false locking has to be prevented.

The sequence of enabling the PFDs at power up is very critical in preventing the false lock. With the detailed schematic of the two PFDs (PFD_Q and PFD_I) illustrated in Fig. 5-(a), let's see how the false locking of the phase rotating PLL can be prevented. Before the CDR circuit starts its operation ($CDR_ENB = \text{HIGH}$), the DLF and PFD_Q are disabled and the phase rotating PLL behaves like a normal PLL with only one PFD/CP pair. Initially the adjacent VCO clocks $\Phi_{VCO}\langle 0 \rangle$ and $\Phi_{VCO}\langle 1 \rangle$ are selected as the feedback clocks Φ_I and Φ_Q , respectively. Therefore, the rising edge of $\Phi_I = \Phi_{VCO}\langle 0 \rangle$ will be locked to that of the input clock Φ_{IN} and then the CDR operation is enabled after this initial phase locking. When the CDR operation begins, initially PFD_Q has to generate UP_Q output because the rising edge of $\Phi_Q = \Phi_{VCO}\langle 1 \rangle$ lags that of $\Phi_I = \Phi_{VCO}\langle 0 \rangle$. When the locking of the rising edge of the feedback clock $\Phi_I = \Phi_{VCO}\langle 0 \rangle$ to that of the input clock Φ_{IN} is completed, the CDR enabling signal CDR_ENB is set to LOW. Because the instant of CDR_ENB going to LOW may be arbitrary, CDR_ENB is latched by the rising edge of $\Phi_Q = \Phi_{VCO}\langle 1 \rangle$, which ensures the PFD_Q is enabled before the rising edge of the input clock Φ_{IN} and after the rising edge

Fig. 6. Microphotograph and layout of the wireline transceiver with the proposed CDR.

Fig. 7. Measured jitter histogram of the recovered clock for 5 Gb/s PRBS data input.

of $\Phi_Q = \Phi_{VCO}\langle 1 \rangle$ as shown in Fig. 5-(b). Thereby, the false locking of the phase rotating PLL can be prevented.

3 Experimental results

The 1.5–5.0 Gb/s wireline transceiver employing the proposed CDR circuit with the phase rotating PLL has been implemented in a 65 nm CMOS logic process and the chip microphotograph and the layout are shown in Fig. 6. The active area of the CDR circuit is 0.17 mm². The main PLL occupies relatively large area but if multiple data lanes are implemented, the portion of the main PLL's silicon area would be reduced because it would be shared among the multiple data lanes. The receiver consumes 22.8 mW from a 1.2 V supply at 5.0 Gb/s data rate.

The jitter histogram of the recovered quarter-rate clock of the CDR circuit is shown in Fig. 7 for 5.0 Gb/s pseudo-random binary sequence (PRBS) serial data input. The peak-to-peak (p-p) and root-mean-square (rms) jitters of the recovered quarter-rate clock are measured to be 28.8 ps and 3.2 ps, respectively.

Table I. Performance Comparison

	[4]	[14]	[15]	[16]	[17]	This work
Process	0.18 μm CMOS	0.13 μm CMOS	65 nm CMOS	0.13 μm CMOS	0.14 μm CMOS	65 nm CMOS
Supply [V]	1.4	1.2	1.2	1.2	1.8	1.2
Data rate [Gbps]	4	5.4	5	10	5.4	5
Area [mm^2]	0.8	1.1	0.51	10.2	0.054	0.17
Power [mW]	14 @ 2-Gb/s	138	178.4	120	22.7	22.8
Clock jitter [psec]	28 (rms) @ 2-Gb/s	5.98 (rms)	N. A.	2.1 (rms)	N. A.	28.8 (p-p) 3.2 (rms)
Jitter tolerance [UIp-p]	N. A.	> 0.22 @ 4-MHz	> 0.3 @ 50-MHz	0.5 @ 4-MHz	4.3 @ 1-MHz	0.21 @ 25-MHz
mW/Gb/s	7	25.55	35.68	12	4.2	4.56

Fig. 8. Jitter tolerance of the CDR circuit at 5 Gb/s.

The CDR circuit is verified to be capable of tracking serial data input with triangular spread spectrum clocking (SSC) up to $-5,000$ ppm spreading and 33 kHz modulation frequency without any degradation in the bit error rate (BER) from its nominal value of 10^{-12} . The jitter tolerance of the CDR circuit is measured as shown in Fig. 8. For the jitter frequency of 25 MHz, the CDR circuit can tolerate up to 0.21 unit-interval (UI = one bit time) jitter for the BER smaller than 10^{-12} . The performance of the proposed CDR circuit with the phase rotating dual-PFD PLL is summarized in Table I.

4 Conclusion

A CDR circuit for 1.5 – 5.0 Gb/s wireline transceiver has been developed in a 65 nm CMOS process. In order to track the phase and frequency difference, a PLL with dual PFD and CP pairs performs the seamless phase rotation for CDR. The receiver consumes 22.8 mW from a 1.2 V supply at 5.0 Gb/s. For the jitter frequency of 25 MHz, the CDR circuit can tolerate up to 0.21 UI

jitter with BER smaller than 10^{-12} . The recovered quarter rate clock has 28.8 ps p-p and 3.2 ps rms jitter.

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