A 2.5-GHz Direct Digital Frequency Synthesizer with spurious noise cancellation

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Abstract: A 2.5 GHz Direct Digital Frequency Synthesizer (DDS) with spurious noise cancellation is presented. Seven auxiliary DDSs have been used as spur cancellers which can generate opposition signal to counteract the spurs in DDS’s output spectrum. Principle of spur cancellation and its implementation scheme is discussed. Key steps of spur cancellation procedure are also described. This DDS is implemented in a 0.18 µm CMOS technology, occupies 4.6 mm × 4.2 mm including bond pads. Measured performance is SFDR > 58 dB for output signal frequencies up to 1 GHz, more than 20 dB’s improvement is achieved comparing to its intrinsic SFDR performance.

Keywords: direct digital frequency synthesizer (DDS), spurious noise cancellation, digital auxiliary for analog design, SFDR

Classification: Integrated circuits

References

1 Introduction

Direct Digital Frequency Synthesizer (DDS) has been widely used in communication and radar systems due to its advantages as high frequency resolution, fast frequency switching, wide tuning bandwidth, low phase noise, arbitrary wave generation, etc. High speed DDS is a mixed signal integrated circuit, its digital blocks can only operate in several hundred MHz (due to digital standard cell’s speed restriction), but the embedded DAC can operate in several GHz, so time-interleaved or interpolation architecture must be used. These architectures would cause the whole circuit has many clock signal (as \(fs, fs/2, fs/4, fs/8\ldots\)), these clock signal would through common substrate coupling, source/ground line induced, bonding wire parasitic effect, generate clock-induced-spurs in DDS’s output spectrum (at position \(\frac{N \cdot fs}{M} \pm K \cdot fout\), \((M = 1, 2, 4\ldots, N, K = 1, 2, 3\ldots\)) as shown in Fig. 1. Most of these spurs in the 1st Nyquist bandwidth, and sometimes these spurs are larger than harmonics which are caused by nonlinear of DAC (at position \(K \cdot fout\), \(K = 2, 3, 4\ldots\)), and determine SFDR performance.

![Fig. 1. DDFS’s output spectrum](image)

Many literatures [1, 2, 3, 4, 5] discuss the ways to reduce spurs, most of them concern about the DAC’s nonlinear (DACs in these literatures doesn’t have many clock signals), or shift part of the harmonics away from 1st Nyquist bandwidth [6, 7]. Literatures [8] presents a high-PSRR current switch for DACs, that method can well suppress clock-induced-spur when signal frequency below 100 MHz, when output signal frequency beyond 100 MHz that method become inefficiency. As the DAC’s clock frequency becomes higher and higher, layout and bonding wire’s parasitic effect becomes more deteriorative, the way to improve DAC’s SFDR becomes more difficult.
This paper’s spur cancellation method can cancel spurs in digital-domain, and has several advantages and disadvantages. The advantages are it is always efficiency and can’t be affected by output signal frequency [9, 10], and it can cancel not only the spurs induced by DDS chip itself but also the spurs induced by the components of the whole transit chain (include balun, power amplifier, mixer). The main disadvantage is that it can only be used when DDS output a steady signal (worked as a high frequency resolution local oscillator, or as a special signal generator for radar system), and when the signal changes the spur cancellation must be redone or uses a look-up table method to change the spur cancellers’ status. This disadvantage limits this method’s application field.

This paper is arranged as follows. Section II briefly presents the overall system architecture of the DDS, Section III presents principle of spur cancellation and also discusses amplitude and phase quantization scheme of auxiliary DDSs (aux-DDSs). Section IV presents the key steps of spur cancellation procedure and measurement result. This paper is concluded in Section V.

2 System architecture

Fig. 2 shows the functional block diagram of this 2.5 GHz DDS which consists of digital block, analog block, clock generator and multiplexer. The DDS core has a 32-bit frequency tuning word [11], and can generate many kinds of signals like linear sweep signal, OSK, FM, AM, etc. To achieve high speed as 2.5 GHz, an interleaved architecture (with interleave factor of 8) has been used which can let the DDS core operates at 312.5 MHz (fs/8).

Seven aux-DDSs which can generate opposition signals to counteract spurs has the same frequency resolution and architecture with DDS core. A
14-bit (5+9) 2.5 GHz DAC has been embedded. Both serial interface and parallel interface are enabled.

This DDS system operates under many different clock frequencies. This will cause clock-induced-spurs in DDS’s output spectrum. Using some layout strategies like separating source/ground line, increasing physical distance, guard-ring, insulated deep-well, etc, would alleviate the clock-induced effect in some degree. But in this 2.5 GHz DDS design, decoder operates at 312.5 MHz which causes input data to the multiplexer is wide (40 bit/channel), that makes a complicate layout and a large instantaneous current. In post-simulation stage, clock-induced-spurs in output spectrum are very serious.

3 Principle of spur cancellation and implementation scheme

3.1 Principle of spur cancellation

In theory, aux-DDSs can generate opposition signals which will counteract any spurs and harmonics in DDS’s 1st Nyquist bandwidth. It need to be concerned that the frequency of opposition signal and target spur must be exactly equal, that means their frequency tuning word must exactly equalize, any minute frequency offset error (even $1/2^{32}$ fs) will cause this method fail.

Opposition signal’s amplitude and phase quantization effect needs to be evaluated. Choosing proper width of quantization will save the chip’s power and area without sacrifice dynamic performance.

Hypothesizing target spur is $A \sin \omega t$, opposition signal is $(A - \Delta A) \sin(\omega t + \pi + \Delta \theta)$, $\Delta \theta$ and $\Delta A$ is the phase error and amplitude error. So cancellation error is Eq. (1):

$$E_r = A \sin \omega t + (A - \Delta A) \sin(\omega t + \pi + \Delta \theta)$$

(1)

The expanded form is Eq. (2):

$$E_r = A \sin \omega t \cdot (1 - \cos \Delta \theta) - A \cos \omega t \cdot \sin \Delta \theta + \Delta A \sin \omega t \cdot \cos \Delta \theta + \Delta A \cos \omega t \cdot \sin \Delta \theta$$

(2)

The term $\Delta A \cos \omega t \cdot \sin \Delta \theta$ can be taken out for it is the high order infinitesimal, so the result is Eq. (3):

$$E_r = A \sin \omega t \cdot (1 - \cos \Delta \theta) - A \cos \omega t \cdot \sin \Delta \theta + \Delta A \sin \omega t \cdot \cos \Delta \theta$$

(3)

If amplitude error $\Delta A = 0$, the cancellation error becomes to Eq. (4):

$$E_r = A \sin \omega t - A \sin(\omega t + \Delta \theta)$$

(4)

Through trigonometric transform the result becomes to Eq. (5):

$$E_r = -A \cos(\omega t + \Delta \theta/2) \cdot \sin \Delta \theta/2$$

$$\approx -A \cos \omega t \cdot \Delta \theta$$

(5)

Eq. (5) shows the cancellation error is linear with phase error which means the character of $6.02 \text{dB/bit}$.

Fig. 3 shows the phase difference versus SFDR when amplitude error is zero.
As Fig. 3 shows, a 8-bit phase quantization will obtain a −40 dB’s SFDR improvement when amplitude error is zero.

From Eq. (3), if phase error $\Delta \theta = 0$, the cancellation error becomes to Eq. (6):

$$E_r = \Delta A \sin \omega t$$

The cancellation error is linear with amplitude error, and also has the character of 6.02 dB/bit.

Fig. 4 shows the effect of amplitude quantization when phase difference is $\pi$ (phase error is zero).

As Eq. (3) shows, if the value of $\Delta \theta$ is small enough, $(1 - \cos \Delta \theta)$ is much smaller than $\sin \Delta \theta$, Eq. (3) can be simplified as Eq. (7)

$$E_r = -A \cos \omega t \cdot \sin \Delta \theta + \Delta A \sin \omega t$$

$$\approx -A \cos \omega t \cdot \Delta \theta + \Delta A \sin \omega t$$

Eq. (7) is just the sum of Eq. (5) and Eq. (6), that means amplitude quantization effect and phase quantization effect are independent if $\Delta \theta$ is small enough.
Fig. 5 shows the combination effect of both amplitude and phase quantization. Amplitude quantization range is \((-1, +1)\) and phase quantization range is \((0, 2\pi)\).

![SFDR vs Amplitude and Phase Quantization](image)

**Fig. 5.** Both amplitude and phase quantization versus SFDR

### 3.2 Implementation scheme of spur cancellation

In circuit implementation, there are several issues need to be considered. The first is that DDS core’s dynamic performance is limited by DAC’s input data width (14 bits), so aux-DDS’s output data width does not need to beyond 14 bits. The second is that spurs are much smaller than DDS core’s output signal, so aux-DDS’s output data width can be less that 14 bits. The third is that it can be seen from Fig. 6, phase quantization width does not need to be much wider than amplitude quantization width for SFDR’s improvement will become saturation.

Fig. 6 shows the implementation scheme of spur cancellation method. DDS core’s output and aux-DDSs’ outputs are LSB aligned, so DDS core’s dynamic performance loss will be negligible. MSB of aux-DDS1 is aligned with the 5th bit of DDS core that will limit the opposition signal’s output range, and DDS core’s output is multiplied by 0.75 to avoid overflow. To ensure the accuracy of aux-DDSs’ outputs, all the Amplitude Scale Factor (ASF) are set to the same width as aux-DDSs’ outputs, and the outputs width of phase to sine converter is set to be 4 bits wider than ASF. Phase Offset Word (POW) and the phase accumulator’s output (32 bits are truncated to 14 bits) are MSB aligned which ensures the tuning range as \((0, 2\pi)\) and make phase tuning resolution as \(2\pi/2^{\text{POW}}\).

Table I summarizes the quantization scheme and performances of every aux-DDS.
Spur cancellation procedure and measurement results

Fig. 7(a) shows the photograph of the 2.5 GHz DDS chip. It was implemented in a 0.18 µm CMOS technology, occupies 4.6 mm × 4.2 mm including bond pads, bonded in a CQFP100 package. Fig. 7(b) shows the test environment, test equipment include: R&S FSUP signal source analyzer, R&S SMA100A signal generator, Agilent DSO90404A digital source oscilloscope and Agilent N6705B DC power analyzer.

The key steps of the spur cancellation procedure shows as follows:

- Read the highest spur’s coarse frequency and coarse amplitude from spectrum analyzer.
- Comparing the coarse frequency with every frequency in the spur lookup table and get the most adjacent frequency as the precise frequency. Spur lookup table is constructed from \( \left( \frac{N \cdot f_s}{M} \pm K \cdot fout \right) \), \( M = 1, 2, 4 \ldots, N \), \( K = 1, 2, 3 \ldots \).

### Table I. Seven aux-DDS’ quantization scheme and performance

<table>
<thead>
<tr>
<th>Aux-DDS</th>
<th>Quantization width</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Phase</td>
<td>Amplitude</td>
</tr>
<tr>
<td>DDS.1</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>DDS.2</td>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>DDS.3</td>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>DDS.4</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>DDS.5</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>DDS.6</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>DDS.7</td>
<td>9</td>
<td>8</td>
</tr>
</tbody>
</table>
Add a small frequency offset (as 1 MHz) to the precise frequency. Then let an aux-DDS to generate a signal using the offset frequency and the coarse amplitude. Tuning amplitude of the aux-DDS till aux-DDS’s output signal and the target spur has the same height on the spectrum analyzer. And then the amplitude of aux-DDS can be considered as the precise amplitude.

Let the aux-DDS generate a signal using precise frequency and precise amplitude, then sweep the phase of the aux-DDS from 0 to $2\pi$. Observe the spur to reach its lowest level. And then the phase of aux-DDS can be considered as the precise phase.

One aux-DDS can only counteract one spur in the spectrum. Spur lookup table must be constructed large enough in order to avoid searching precise frequency failed. Negative frequency in the lookup table must use its absolute value. Phase sweep can use optimized method for fast search.

Fig. 8 and Fig. 9 shows spectrum analyzer screenshots of 49 MHz and 999 MHz output signal, each frequency shows an intrinsic performance and a spur cancelled performance.

Fig. 10 shows the measured SFDR versus output frequency.

Fig. 11 to Fig. 12 shows phase noise curve and time-domain waveform. Table II summarizes the measured performance.
From the measured results, the intrinsic SFDR performance of the 2.5 GHz DDS is worse than most of the literature, that may partly because of poor layout and serious package parasitic effect. The digital spur cancellation method improved more than 20 dB for SFDR. It is need to be reminded that spur cancelled SFDR is determined by the highest spur which never be counteracted, all the spurs which had been counteracted were lower than –70 dBc. In the future, this DDS will be optimized in two aspects, the first is
Fig. 12. Time-domain capture of output signal

Table II. Measured performance of the 2.5 GHz DDS.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Measured results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>3.3 V/1.8 V</td>
</tr>
<tr>
<td>SFDR@49 MHz</td>
<td>53.21 dB (intrinsic)</td>
</tr>
<tr>
<td>SFDR@999 MHz</td>
<td>28.19 dB (intrinsic)</td>
</tr>
<tr>
<td>Phase noise@49 MHz</td>
<td>–130.08 dBc/Hz@10 kHz</td>
</tr>
<tr>
<td>Phase noise@999 MHz</td>
<td>–109.62 dBc/Hz@10 kHz</td>
</tr>
<tr>
<td>Power consumption@999 MHz</td>
<td>1.9 W (aux-DDS disabled)</td>
</tr>
</tbody>
</table>
to optimize layout and try smaller size package for better intrinsic SFDR, the second is to add more aux-DDSs to counteract more spurs. If all this optimization design steps had been done, an extra 10 dB’s SFDR improvement will be expected.

5 Conclusion

This paper presented a digital spur cancellation method in a 2.5 GHz DDS. Seven aux-DDSs which act as spur cancellers have been used to generate opposition signal to counteract spurs in DDS’s output spectrum. This method works in digital-domain, not interrelated with output signal frequency. The DDS is implemented in a 0.18 µm CMOS technology, achieves a SFDR > 58 dB for output signal frequencies up to 1 GHz. Comparing to its intrinsic performance, this method has improved DDS’s SFDR for more than 20 dB.

Acknowledgments

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