An 180 nm CMOS 1.84-to-3.62 GHz fractional-N frequency synthesizer with skewed-reset PFD for removing noise-folding effect

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Abstract: To remove the noise folding effect, which is a primary cause of degradation of the close-in phase noise of fractional-N phase-locked loops (PLLs) that use sigma-delta modulation, a fractional-N frequency synthesizer for broad-band and multi-standard mobile TV tuners was designed. The proposed skewed-reset phase frequency detector (SR-PFD) provides a key solution to the problem of noise folding by enhancing the linearity of the phase frequency detection path through the charge pump (CP). Degradation of the reference spur—the unwanted effect in SR-PFDs—is blocked through the use of a sampled loop filter. An SR-PFD in a frequency synthesizer fabricated on a 180 nm CMOS process enhanced phase noise by 10 dB or more by using a multi-stage noise shaper (MASH) 1-1-1 sigma-delta modulator (SDM), while a sampled loop filter decreased the amplitude of the reference spur by 7–13 dB.

Keywords: fractional-N frequency synthesizer, mobile TV tuner, noise folding effect, sampled loop filter, skewed-reset PFD

Classification: Integrated circuits

References

1 Introduction

Broad-band frequency synthesizers used in multi-band mobile TV tuners for receiving FM, terrestrial digital multiband (T-DMB), digital video broadcasting-handheld (DVB-H), and integrated services digital broadcasting-terrestrial (ISDB-T) signals have strict close-in phase noise requirements for accurate demodulation [2, 4].

In many cases, however, the fractional-N phase-locked loops (PLLs) in synthesizers suffer from a noise-folding effect that increases the close-in phase noise spillover from the high-frequency portion of the sigma–delta modulation (SDM) quantization noise because the PLLs are generally locked at the most nonlinear point (0° when using a three-state PFD) in the transfer function from the phase frequency detector (PFD) through the charge pump (CP). A simple and effective technique for blocking the effect of noise folding is to move the locking point to more linear regions of the transfer function; this can be implemented in a straightforward manner by making a current offset between UP and DN in the CP [1] in which the phase offset is determined by the ratio between the CP and offset currents. Another solution is to phase offset the PFD instead of the CP [2, 3]. One uses a modified three-state PFD that is designed to adopt the reset signal from only the reference-originated clock in order to ensure that the reference clock leads the divider clock by the phase offset while locked. As PLLs cannot be used for phase acquisition using this architecture, they should be switched to conventional PFDs during the acquisition. In addition, operational failure can occur during multi-bit SDM because this procedure produces flat gains at negative input phase. The other one is to skew the reset delay to UP/DN D-flip-flops by the required phase error, and thus it effectively adds the phase error. This scheme works in the same way as the technique of the current offset does, while it avoids static current consumption. But, it adds the fixed phase error to the divider-side flip-flop in a unidirectional way. The common problem from such the noise folding avoidance schemes is that those increase the reference spurs with the repetitive charging and discharging by the phase offset.

In this paper, we propose a new PFD scheme with a bidirectional skewed reset control. The proposed circuit implements phase offsetting without distorting the transfer function and can change the direction and magnitude of offset using simple controls. Also, to avoid the problem of phase offset-induced reference spurs, we designed a sampled-loop filter in which the sampling time duration is adaptively changed based on the CP turn-on time in order to minimize the transfer of device noise.
2 Circuit implementation

Fig. 1 shows a block diagram of the proposed frequency synthesizer for a multi-standard mobile DTV tuner. The synthesizer consists of a skewed-reset phase frequency detector (SR-PFD), a charge-pump (CP), a third-order loop filter with two sampled capacitors (C1a and C1b) and a tunable capacitor (C3), an LC VCO that operates in the range 2400–3600 MHz, an N divider designed with a modular counter, and a multi-configurable sigma-delta modulator (SDM) employing multi stage noise shaping (MASH) 1-1-1 and a third-order interpolative SDM.

Because the SR-PFD increases the reference spur, we designed a sampled loop filter to block the redundant charge transfer caused by the phase offset. To perform this operation, switch S1 disconnects C1a from the remaining loop filter while the CP is functioning; after the CP stops, C1a is turned on in order to distribute its charge to C1b.

A. Skewed-reset PFD (SR-PFD) & switch controller

Fig. 2 shows the proposed SR-PFD and the switch controller for the loop filter. As seen in Fig. 2(a), the SR-PFD is designed to split the reset signals sent to DFF1 and DFF2 into R1 and R2 in order to produce four different delay options depending on the four possible bit combinations produced by SELR and SELD together.

Production of the common sets (0,0) and (1,1) by \((SEL.R, SEL.D)\) causes both R1 and R2 to be delayed from R0 by \(\tau_1\) and \(\tau_1 + \tau_2\), respectively, while (0,1) among the other skewed-delay options cause the R0-to-R1 delay to be \(\tau_1\) and the R0-to-R2 delay to be \(\tau_1 + \tau_2\) (and vice-versa for (1,0)). The switch controller shown in Fig. 2(b) generates a pulse in order to determine the duration of switch connection for the sampled loop filter. The flip-flops of DFF3 and DFF4 are reset and \(\phi_{DIV_p}\) is returned to “LOW” only if \(R.UP\) and \(D.DN\) are commonly “LOW” Fig. 2(c) shows a sample waveform with \((SEL.R, SEL.D)\) set to (0,1). If DFF1 is first triggered by \(\phi_{REF}\), \(R.UP\) goes “HIGH”, if the pulse \(\phi_{DIV}\) follows, a reset signal is generated on \(R0\), which is
delayed relative to $R1$ and $R2$ by $\tau_1$ and $\tau_1 + \tau_2$, respectively. Because $R_{UP}$ and $D_{DN}$ are reset by $R1$ by $R2$, respectively, the delay between the falling edges of the two pulses equals $\tau_2$. In the switch controller, the falling edge of $D_{DN}$ triggers $RT$ “HIGH” and after a delay of $\tau_C$, $dRT$ goes “HIGH” as well. Using this design, the on-time duration of $LF_{SW}$ can be made adaptively variable depending on the turn-on time of the CP, compared with the fixed duration used in previous designs [1].

**B. VCO**

Fig. 3 shows a detailed schematic diagram of the designed VCO, which targets the frequency range from 2.4 to 3.6 GHz with sufficient margin. To cover this broad frequency range, we designed a capacitor bank composed of seven-bit binary-segmented capacitors for coarse tuning; for fine tuning, we designed three accumulation metal-oxide semiconductor (AMOS) varactors biased to the low, mid, and high voltages ($V_{b3}$), ($V_{b2}$), and ($V_{b1}$), respectively, to extend the usable range of fine tuning to the boundary ranges around GND and VDD.
C. SDM (Sigma-delta modulator)

In general, a higher order sigma-delta modulator (SDM) with more output bits will have a greater impact on noise folding. To implement this design, we chose to use the MASH 1-1-1 SDM, which has three-bit outputs and a third order noise transfer function (NTF).

However, this SDM has the largest quantization noise power at $f_{\text{ref}}/2$ in the NTF of any third-order SDM. Furthermore, the use of a divider-by-two in front of the SDM doubles the total quantization noise. For comparison purposes, we designed a multi-configurable SDM that can be selectively configured between the MASH 1-1-1 and third-order interpolative types. The third-order interpolative SDM option can be employed to lower the high-frequency quantization noise by moving the corner frequency of the NTF downward in order to reduce the noise folding effect.

3 Experimental results

Fig. 4 shows a microphotograph of the fabricated frequency synthesizer on a 180 nm CMOS process. The chip occupies an active area of 0.33 mm$^2$ and
consumes an average power of 25.34 mW with a 1.8-V supply voltage. The oscillation frequency of the standalone VCO was measured to range between 1.84 and 3.62 GHz, which can support broadcasting tuners for receiving FM, VHF-III, UHF, and European L-band transmission.

Fig. 5 shows a plot of phase noise measured from the synthesizer’s output. It is seen in Fig. 5(a) that the excessive quantization noise from the MASH affects even the out-band noise (Curve A), and it is seen that the contribution of the noise beyond the loop bandwidth is removed when the tunable third pole caused by R2 and C3 is reduced to minimum (Curve B), although this does not work for noise folded into the loop bandwidth. When the SR-PFD is turned on in the following step, the in-band phase noise is removed (Curve C). Fig. 5(b) shows another case of phase noise demonstrating the effects of using SR-PFD vs. integer mode phase noise.

Fig. 5. SSB phase noise (a) Reduction of MASH 1-1-1 noise by tuning of the third pole and the SR-PFD (b) Reduction in noise folding by using SR-PFD vs. integer mode phase noise
quantization noise from MASH 1-1-1 is fully removed when the SR-PFD is turned on; this result closely matches Curve C obtained with the SDM off, although, in the latter case, the out-band noise is not fully filtered by the third pole. Fig. 6 shows the phase noise measured using the third-order interpolative SDM; as expected, it is seen here that the in-band phase noise less degraded owing to a smaller noise folding effect. However, scaling the corner frequency down contributes more to the measured out-band phase noise. These results lead is us to conclude that the proposed SR-PFD successfully reduces the noise folding effect to the level found in an integer PLL; as such, it can be used to implement comparative fractional-N PLL that meets in-band phase noise requirements even when using a MASH 1-1-1. Fig. 7 shows that, by using a sampled loop filter, the reference spur is reduced to 13.1 dB when the reference clock is divided by two.

Table I summarizes comparison results with recent DTV tuner frequency synthesizers. For fair comparison of the in-band phase noise, the following normalization was applied.

\[ PN_{\text{norm}} = PN_{\text{meas}} - 20 \log\left(\frac{f_{\text{meas}}}{f_{\text{ref}}}\right) - 10 \log(f_{\text{ref}}) \]  

(1)

Fig. 6. Noise folding by third-order interpolative type SDM and the effects of noise reduction by the SR-PFD

Fig. 7. Reference spur reduced by using the sampled loop filter
4 Conclusion

As the proposed SR-PFD and sampled loop filter enables the attainment of low-level close-in phase noise and smaller reference spurs, it produces a corresponding enhancement of phase error or error vector magnitude (EVM). A PLL fabricated on a 180 nm CMOS process demonstrated 10 dB or more reduction in the in-band phase noise and 7–13 dB enhancement in the reference spur relative to a basic PLL scheme without an SR-PFD.

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<th>Table I. Performance summary and comparison</th>
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<td>Meas. Freq. [GHz] 3.404</td>
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<tr>
<td>PN [dBc/Hz]</td>
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<tr>
<td>$PN_{\text{meas}}@10\text{kHz}$ -88 (-205.8) -102 (-195.6) -93 (-195.8) -84 (-201.5)</td>
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<td>$PN_{\text{norm}}$</td>
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<td>$@1\text{MHz}$ -111 -119 -119 -115 -126</td>
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<td>Worst-case Spur [dBc] -62.8 -74 -61.2 N.A. N.A.</td>
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