A 1.1 mW/Gb/s 10 Gbps half-rate clock-embedded transceiver for high-speed links in 65 nm CMOS

Kyongsu Lee^{a)}, Youngjin Kim, Kyungsub Son, Sangmin Lee,
and Jin-Ku Kang

*Electronic Engineering Dept., Inha University,
100 Inharo, Nam-gu, Incheon, 402–751, South Korea
a) kyungsul@inha.ac.kr*

Abstract: This paper presents a low-power half-rate clock-embedded transceiver architecture that employs quarter-rate multiplexing/de-multiplexing circuit technique, low-V_{dd} current-mode driver topology embedding half-rate clock, and multi-functional injection-locked oscillator (ILRO) for a digital clock and data recovery (CDR) design. The whole transceiver circuit was simulated in 65 nm CMOS process and its feasibility was proved successfully operating at 10 Gb/s across a band-limited channel. The achievable power efficiencies of the receiver and transceiver were 0.7 mW/Gb/s and 1.1 mW/Gb/s respectively.

Keywords: CDR, ILRO, clock-embedded transceiver, high-speed links

Classification: Integrated circuits

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1 Introduction

Conventional clock and data recovery (CDR) techniques make use of transition edges of received data for the clock recovery in high-speed links. When a reference clock is provided at receiver, a phase-locked loop (PLL) is used to generate clock frequency and align its phase onto the edges of data. This technique often requires transition coding in the data stream to permit enough transition information for the clock recovery, which reduces signal transmission efficiency. Often, a second-order loop has to be implemented to decrease any frequency offset between transmitter clock and reference in the receiver complicating CDR design [1]. Without a reference, receiver clock still can be recovered at the cost of complexity in the design, area, and power [2].

Recently, clock-embedded signaling schemes [1, 3, 4] have been introduced and proved their feasibilities for high-speed links. In these techniques, a transmitter clock is combined with data and is sent over the same channel as the transmit data. The extracted clock at the receiver can be used as a reference for the data recovery. By this way, no additional wire for the clock is needed and frequency offset can be removed as well.

In this paper, we propose a power-efficient transceiver architecture for clock-embedded signaling in which a half-rate clock is commonly combined with each of differential data at transmit driver and recovered to generate 8-phase sampling clock for the 1:4 de-multiplexing in the receiver. To alleviate matching issues in the channel [3], a digital bang-bang CDR scheme is implemented to track data transitions instead of source-synchronous delay-matching scheme used in [3, 4].

2 Transceiver architecture

Fig. 1. Basic concept of the proposed transceiver.

The basic concept of proposed transceiver is described in Fig. 1. In the transmitter, a differential data signal is driven by 4:1 multiplexing pre-drive retimed by 4-phase clock. At the driver output, each leg of differential data is combined with a single-phase half-rate clock, which is synthesized from 4-phase quarter-rate clock, and transmitted across band-limited channel. A continuous time linear equalizer (CTLE) recovers differential data by subtraction and amplifies high-frequency band of data spectrum to compensate for the loss from the channel. The clock recovery can be easily achieved by using common-mode amplifier (CMA) [3], which rejects differential-mode data signal during the amplification. The recovered differential clock is divided and used as reference input for the 8-phase quarter-rate clock generation. Since the reference clock is provided, the digital CDR requires only 1st-order phase detection loop eliminating the need for frequency acquisition

loop. For low power consumption, most of proposed transmitter and receiver circuits in the following discussions are implemented with low supply voltage (0.8 V) in 65 nm CMOS process.

Fig. 2. Proposed transmitter concept operating at 10 Gb/s.

2.1 Transmitter circuit

For low power operation at 10 Gb/s, the proposed transmitter employs 4:1 multiplexing and low- V_{dd} current-mode driver as shown in Fig. 2. For the 4:1 multiplexing, each of four pre-driver generates a sequential pulse from two neighboring phases supplied from 4-phase clock source and drives each of 2.5 Gb/s input to the data driver during the high-level of the pulse, which corresponds to 1 UI of data transmission. In the proposed Tx scheme, a half-rate clock (5 GHz) should be added at the output of Tx driver. For this purpose, a half-rate clock is synthesized by combining the outputs of two pulse generators where each pulse is spaced by 90° and its width is 45° of 2.5 GHz clock. The driving strength of the clock driver is designed about half of data driver and its phase is cautiously adjusted to minimized inter-symbol interference (ISI) of combined signal in the presence of band-limited channel [3]. This half-rate clock is combined at each leg of differential data at the transmitter output.

Voltage-mode driver is desirable for low power transmitter because it does not dissipate static current. However, its output common-mode (CM) level is closely coupled with output impedance. For example, when NMOS push-pull stage is employed [5], output CM level should be close to ground to allow switching operation of its pull-up NMOS transistor. As a result, it prevents receiver front-end from using high-bandwidth NMOS transistors. If pull-up transistor is replaced with PMOS, then complementary pre-driver stage is additionally needed, which increases design complexity.

In the proposed transmitter (Fig. 3), current-mode (CM) driver with resistive load is employed to satisfy high-bandwidth receiver requirement. The load resistance is shared with 4 data drivers in parallel to accomplish 4:1 multiplexing. The synthesis of half-rate clock is achieved by merging two clock drivers where each of pulling-down pulse is spaced by 90° of 2.5 GHz. The amplitude ratio of data to clock is determined by the 2:1 ratio of their current sources [3].

Fig. 3. Differential current-mode drivers implementing 4:1 data multiplexing and half-rate clock synthesizing.

2.2 Receiver circuit

Fig. 4. Proposed receiver operating at 10 Gb/s.

The differential data signal can be separated from common-mode clock signal by simple subtraction operation in the CTLE circuit (Fig. 4), which is typical source-regenerative topology followed by differential pair [3]. The band-pass filtering function of CTLE compensates loss of high-frequency energy of data signal filtered out by the band-limited channel. The following 1st-order digital CDR consists of quarter-rate octave-phase bang-bang detector, decimator, FSM, and 6-b accumulating counter. The 4-way time-interleaved PD requires 8 phases of quarter-rate (2.5 GHz) clocks for the bang-bang phase detection i.e. 4 phases for the data sampling and the other 4 phases for the edge detection. The 8 early/late data from the PDs are inputted to the decimation circuit [6] to vote UP/DN direction for the counter. The FSM block controls enable timings of the loop (i.e. injection and counter) and loop bandwidth by choosing clock division ratio. The two selection bits (SELDV[0:1]) determines 4 clock division ratios (2, 4, 16, and 32) between DVCK8 and CCK. When sinusoidal input jitter (Φ_{IN}) is assumed, loop bandwidth of digitally controlled CDR with bang-bang PD is defined as [7]

$$\text{Loop bandwidth} \approx \frac{1}{2\pi \cdot \Phi_{IN}} \cdot \alpha_d \cdot \frac{\Delta T}{DF \cdot T_{sck}} \quad (1)$$

where ΔT is step resolution of delay element, α_d is transition density, DF is decimation factor, and T_{sk} is update period of state machine. Based on the UP/DN direction, the counter increases or decreases its 6-b binary code, which is used for controlling the phase of sampling clock.

The CMA amplifies embedded half-rate clock signal (5 GHz) while rejecting differential signal. An inductive-load CMA topology [3] in Fig. 5 is used to achieve more than 10 dB of common-mode gain. The differential mode signal, i.e. data, is canceled out by short-wired output of the amplifier while common-mode signal, i.e. clock, is boosted by shunt capacitor (C_M). The single-ended output of CMA is

converted to differential clock by the following single-to-differential (S2D) converter. In this paper, common-source common-drain S2D converter topology [3] is selected and optimized for low VDD operation. The following limiting amplifier converts small-swing S2D output to rail-to-rail swing. The half-rate differential clock is converted to quarter-rate 4-phase clock by the frequency divider.

Fig. 5. Clock recovery circuit in the receiver front-end.

For 1:4 multiplexing of received data, the bang-bang PD should have 8 samplers, which are driven by 8 quarter-rate clock phases, to provide data and edge information. In the proposed receiver, injection-locked ring oscillator (ILRO) is used to generate eight-phase clock from the four-phase clock input. The ILRO (Fig. 6) consists of four differential inverting stages where each output is cross-coupled to each other. If the free-running frequency of oscillator is close to quarter-rate frequency (2.5 GHz), injection locking can be achieved by turning on the switch (injon). As a result of injection, the oscillator frequency is locked to the injection clock frequency and each phase output is spaced by 45° [8].

The second important advantage of employing ILRO is its phase tuning capability, which obviates the use of delay-line in the CDR loop. For this purpose, the oscillation frequency of ILRO after locking is tuned digitally by 6-b capacitor bank at each node. The 6-b phase tuning code (B[0:5]) is generated from the accumulating counter in Fig. 4, thereby completes phase tracking loop of CDR. The maximum tuning range must at least cover 1UI (i.e. 100 ps for 10 Gb/s) of data transmission, corresponding to $\pm 45^\circ$ of quarter-rate clock, which can be easily achieved by the injection-locking [8].

The third important advantage of using ILRO is its jitter filtering capability of injected signal just like 1st-order PLL where its 3 dB frequency is defined by the locking range [8]. As we discussed in detail in the reference [3], the addition of weak clock signal with differential data at Tx causes data dependent jitter (DDJ) in the clock signal. Because of limited Q-factor of BPF and differential-mode rejection gain of receiver front-end circuits, the high-frequency DDJ can still remain in the extracted clock signal. Therefore, the use of ILRO helps to filter out this remaining DDJ outside its 1st-order bandwidth.

Fig. 6. A differential 4-stage injection-locked ring oscillator to generate tunable octave-phase clock.

3 Experimental results

The proposed transmitter and receiver circuits are implemented in 65 nm CMOS process and interconnected with 5'' PCB trace. The simulated waveforms at receiver front-end at 10 Gb/s data rate are shown in Fig. 7. The Rx input waveform includes 10 Gb/s data and 5 GHz common-mode clock. From this Rx input, differential signal, which is denoted by EQ output, is extracted and equalized in the data recovery. In the clock recovery, only the common-mode clock signal (CMA output) is extracted and amplified by CMA. A single-ended CMA output is converted to the differential (S2D output) by the S2D converter and limiting amplifier. The following differential divider converts differential clock to quad-phase clock of quarter-rate frequency (2.5 GHz).

The eye diagrams of Rx input and equalizer output for 10^3 symbols are compared in Fig. 8. When 5-inch PCB (FR4) trace is used to interconnect transmitter and receiver, the eye (less than 100 mV) of received signal (Fig. 8a) is almost closed due to the significant ISI. After equalization, the eye (> 450 mV) of equalizer output (Fig. 8b) is wide opened and common-mode signal is removed. The CMA output accumulated for 500 clock cycles is also shown in Fig. 8c. The peak-to peak jitter is about 5.3 ps.

Fig. 7. Signal waveforms at the receiver front-end (10 Gb/s).

Fig. 8. Eye diagrams of a) Rx input and b) equalizer output signals at 10 Gb/s, and c) accumulated CMA output at 5 GHz.

The BPF of CMA can filter out the most of DDJ in the extracted clock signal. However, due to the limited Q-factor (< 5) of the BPF, the CMA output still includes remaining DDJ. Also, the following S2D converter, limiting amplifier, and divider circuit may contribute power noise induced jitter to the injection clock. The ILRO bandwidth defined in eq. (1) is designed around 300 MHz to filter out clock jitter. The peak-to peak jitter of the injection clock and the ILRO output is compared in Fig. 9 when 50 mV power noise of 500 MHz is added for the experimental purpose. About 29% reduction of jitter accumulated for 250 clock cycles is achieved by the injection locking.

The 8 banks of bang-bang PDs require 8 equally spaced clock phases to accurately detect the phase position information. Thus, any phase-offset error between neighboring phases contribute sampling margin reduction or BER increment. Therefore, mismatches between injection ports and non-injection ports of the ILRO should be tightly controlled. For this purpose, we supplied common-mode DC (V_{cm} in Fig. 6) to the non-injection ports to reduce phase offsets. The equally spaced ILRO output of 8-phase clock is shown in Fig. 10 where phase-offset error is less than $\pm 1^\circ$ of 2.5 GHz clock.

Fig. 9. Peak-to-peak jitter of a) the injection clock and b) ILRO output clock in the presence of power noise.

After injection locking, the output frequency of ILRO is locked to the injection frequency. Tuning the phase of output clock can be achieved by modulating 6-b binary code (B[0:5] in Fig. 6), for integrated capacitor banks which in turn changes

internal resonance frequency [8]. For the quarter-rate bang-bang phase detection, each sampling clock must cover $\pm 0.5\text{UI}$ of symbol data rate (10 Gb/s). Thus, the tunable range by 6-b code should be larger than 1UI (100 ps at 10 Gb/s). Fig. 11 shows that the proposed ILRO with 6-b capacitor bank covers more than 1UI and keeps good linearity within the range. It also shows that phase-offset error between the two neighboring phases (P0 and P45) is negligible within the operation range. The average resolution per counting step is about 2.5 ps.

Fig. 10. Eight equally spaced ILRO output clocks after injection locking.

Fig. 11. Proposed ILRO phase delay according to control code.

The functionality of the CDR loop is tested when Rx is connected to Tx across 5-inch trace. At 10 Gb/s data rate, the receiver CDR tracks incoming data transitions and locks successfully at the optimal phase for the sampling. Fig. 12 exhibits UP/DN direction inputs for 6-b counter, its counting clock (CCK) at 2.5 GHz/32 rate, and binary code (B[0:5]). When the injection is enabled, the counter starts down counting based on the output of decimator (i.e. DN = high). During this phase tracking period, decrement of digital code increases phase delay of ILRO output (or sampling clock). When the edge clock (P45, P135, P225, and P315 in Fig. 6) aligns with data transition (i.e. locking period), the counter stops

down counting and starts toggling up and down. In this toggling period, only the LSB (B[0]) of 6-b code is up and down as shown in Fig. 12 contributing 7.2ps dithering jitter.

Fig. 12. Closed-loop CDR locking behavior at 10 Gb/s.

The power consumptions of transceiver circuits are summarized in Table I. Compared to previous similar works as shown in Table II, the proposed receiver achieves significantly lower power (0.7 mW/Gb/s) while the whole transceiver consumes 1.1 mW/Gb/s at 10 Gb/s.

Table I. Power breakdown

Transmitter	3.7 mW @10 Gb/s
Receiver	7.4 mW @10 Gb/s
Clock recovery front-end	3.7 mW
Data recovery front-end	0.8 mW
CDR loop	2.9 mW
ILRO	2.1 mW
Total	11.1 mW @10 Gb/s

Table II. Comparison with prior-art receivers

Reference	*This work	[1]	[3]	[4]
Signaling	1 link + CM clock	1 link + DM clock	1 link + CM clock	2 links + DM clock
Sampling clock	Quarter-rate	Full-rate	Half-rate	Half-rate
Clock phase tuning scheme	CDR	CDR (manual)	Matched delay	Delay-line in Tx
Supply [V]	0.8/1.2**	1.5	1.3	N/A
Max. data rate [Gb/s]	10	5	9	5
Technology	65 nm	130 nm	130 nm	40 nm
Power efficiency [mW/Gb/s]	0.7	3.5	3.1	5.3

*. Circuit simulation results.

**. 1.2 V applied only for high-speed samplers and clock buffers.

4 Conclusions

A power-efficient transceiver scheme for half-rate clock-embedded signaling is proposed. Low-power techniques include quarter-rate multiplexing/de-multiplexing scheme, low-V_{dd} current-mode driver logic embedding half-rate clock, and multi-functional ILRO circuit that greatly simplifies receiver design. The major functions of digitally controlled ILRO in the 1st-order digital CDR loop are to generate equally spaced 8-phase clock for the bang-bang phase tracking loop, to tune 1UI of sampling clock phase eliminating the need for delay-line, and to filter out remaining DDJ in the extracted clock. The proposed transceiver was simulated in 65 nm CMOS process and proved the feasibility of the concept by operating successfully at 10 Gb/s. The achievable power efficiency of receiver (0.7 mW/Gb/s) was much less than previous works with similar signaling schemes. The whole transceiver consumes 1.1 mW/Gb/s at 10 Gb/s.

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