A fast and efficient automatic frequency calibration technique for 10 GHz PLLs

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Abstract: A fast and efficient automatic frequency calibration (AFC) technique suitable for high frequency PLLs is presented in this paper and a 10 GHz PLL using the proposed AFC circuit is designed in 65nm CMOS technology. The fast AFC technique is achieved through a multi-phase clock sampling based algorithm which reduces comparison time of each calibration step to at least one reference cycle with small frequency resolution. A dual-mode frequency divider is proposed to save circuit cost for a high frequency multi-phase clock generator. The proposed divider generates 8-phase high frequency clock for the proposed AFC to reduce its calibration time. Simulation results demonstrate that the calibration time is less than 1.44μs for each output frequency. The proposed AFC circuit is competitive among published AFC techniques in calibration time, unit cycle frequency resolution, area cost and power dissipation.

Keywords: fast frequency calibration, high frequency PLL, dual-mode frequency divider

Classification: Integrated circuits

References

1 Introduction

Automatic frequency calibration (AFC) is a very important digital building block of frequency synthesizer because it breaks the trade off between frequency tuning range and phase noise. By using AFC circuit and N-bit capacitor bank based voltage controlled oscillator (VCO) [1], frequency tuning range is distributed from a single tuning curve to $2^N$ tuning curves, which largely reduces up-converted VCO phase noise by reducing $K_{VCO}$ [2]. However, calibration time is a major concern of PLL settling time because its time cost is larger than the analog part of PLL lock time.

All reported AFC techniques have their own disadvantages. Relative frequency comparison algorithm AFC (counter based) is time inefficient due to its long comparison time [3] and low comparison resolution [4]. Time-to-voltage converter based relative period comparison algorithm is the fastest calibration circuit ever reported [5, 6]. However, since it is based on analog voltage comparator, its frequency resolution suffers a lot from analog circuit mismatch, which cannot be avoided during circuit implementation. Another drawback of analog AFC is its steady state power dissipation, which adds to PLL total power consumption. A fast digital calibration algorithm is introduced in [7] by increasing clock frequency of counter based AFC, but a high frequency divider is needed to generate high frequency clock signal for AFC, which is power and area costly. This paper aims at designing a fast AFC circuit with the least area cost and power dissipation.

In this article, a fast and efficient AFC technique using multi-phase sampling algorithm in cooperating with a dual-mode divider is introduced, which achieves high calibration accuracy with the minimum achievable calibration time of only one reference cycle for each comparison, without circuit cost for high frequency clock generation.

This paper is organized as follows. Section II introduces the architecture of the proposed frequency synthesizer and describes the principle of the proposed fast calibration algorithm. Section III shows circuit implementation of the proposed dual-mode frequency divider, which can be used as a multi-phase high frequency clock generator during AFC transient. Section IV demonstrates advantages of the proposed frequency synthesizer through simulation results. Section V summarizes this paper and draws a conclusion.

2 Proposed VCO frequency calibration technique

Architecture of the proposed frequency synthesizer is shown in Fig. 1. The synthesizer has two modes, N and M, which are correspond to the mode of the frequency divider. PLL operates at N mode during steady state while its output frequency is decided by divide ratio N. It operates at M mode during AFC transient while the frequency divider’s division ratio M is much smaller than N. In M mode, divider provides high frequency clock signal for digital AFC circuit ($f_{afc} = f_{vco}/M$)
and the AFC generates 6-bit coarse tuning word for VCO capacitor bank. The divide-by-M step reduces VCO frequency to be an available clock for digital circuits and generates 8-phase \( f_{afc} \) for AFC, which facilitates the multi-phase sampling technique to accelerate AFC speed.

As is shown in Fig. 1, VCO calibration is a counter based 6-bit binary search process \((V_{ctrl}[5:0])\) with a clock frequency of \( f_{ref} \). Reference signal \( f_{ref} \) decides counting time \( kT_{ref} \) of each binary step and the number of \( f_{afc} \)’s rising edge is counted and recorded as \( D_{cont} \). Analysis in [7] calculated the achievable comparison precision \( f_{resolution} \) of digital counter based AFC, given by

\[
f_{resolution} = \frac{M \cdot f_{ref}}{k}
\]

This multi-phase clock sampling technique improves calibration resolution by a factor of 8 without increasing clock frequency. During each comparison, rising edge of \( f_{afc}(0^\circ) \) is counted within a time of \( kT_{ref} \) and phase information of clock phases \((0^\circ, 45^\circ \cdots 315^\circ)\) is sampled by \( f_{ref} \) at the start and the end of counting. Sampled results are recorded as the start case \( (C_s) \) and end case \( (C_e) \). Number of \( C_s \) and \( C_e \) value \((0 \sim 7)\) and the corresponding sampled phase position are shown in Fig. 1. Effective counter value \( D_{eff} \) is calculated as follows

\[
D_{eff} = 8 \times D_{cont} + C_e - C_s
\]  

\( D_{eff} \) is compared with the desired counter value \( D_{target} \) at the end of each comparison step. The target output frequency is decided by \( D_{target} \) which should be set before calibration, given by
\[ D_{\text{target}} = \frac{k \cdot T_{\text{ref}}}{T_{\text{target}} / M} \]  

(3)

\( T_{\text{target}} \) is the period of the desired PLL output signal.

The sign bit of counting error \( D_{\text{err}} \) (\( D_{\text{err}} = D_{\text{eff}} - D_{\text{target}} \)) decides searching direction of the next binary step. The value of \( D_{\text{err}} \) and its corresponding capacitor bank code are stored in the optimal final code register after each comparison and will be updated if the newly calculated \( D_{\text{err}} \) is smaller. While all 6 comparison steps finish, capacitor bank code with the minimum \( D_{\text{err}} \) is chosen for VCO.

Since \( C_s \) and \( C_e \) in equation (2) provide the period information of \( T_{\text{afc}} / 8 \), the frequency calibration resolution \( (f_{\text{resolution}}) \) can be improved by 8 during the same calibration time, which reduces the counting time by a factor of 8.

### 3 Dual-mode frequency divider

Since the high frequency multi-phase clock generator is a power hungry and area costly circuit, a dual mode divider topology is proposed to embed the clock generator in steady state divider to save power and area cost. Topology of the proposed multi-stage divider is shown in Fig. 2. Each stage is made up of a \( 2/3 \) divider which is composed of D-latches and logic gates [8].

![Fig. 2. Architecture of the proposed frequency divider](image)

Divide ratio \( N \) and \( M \) correspond to PLL operation state, as introduced in section 2. \( N \) and \( M \) selection is decided by the connections between stage 2 and stage 3, as shown in Fig. 2. \( N \) mode is used at steady state and the divider is a conventional multi-stage divider in \( N \) mode. The divide ratio \( N \) is controlled by \( R_1 \sim R_7 \), given by

\[ N = 2 \times (2^7 + 2^6R_7 + 2^5R_6 + 2^4R_5 + 2^3R_4 + 2^2R_3 + 2R_2 + R_1) \]  

(4)

The range of \( N \) is 256–510 which supports the desired frequency range of 9.5–12 GHz, with 25 MHz reference frequency.

Fig. 3 shows the circuit implementation of each \( 2/3 \) stage of the multi-stage divider, in which stage 2 can be switched to an 8-phase clock generator at \( M \)-mode. In this design, TSPC (True Single Phase Clock) logic is used to implement D-latches of stage 1 and 2 to reduce their power and area consumption compared to conventional high frequency current mode logic (CML) topology D-latches. Logic functions are embedded in D-latches to minimize their power consumption.
M mode is used at AFC transient for multi-phase high frequency clock generation. The required M is 16, which is not in N’s range (256–510). As a result, a circuit modification should be performed to provide a divide ratio of 16.

In M mode, stages 0∼2 are utilized while stages 3∼7 are inactive. Divide ratio of stage 1 is set to 2 by grounding R1. R2 and M2 are tied high and the mode control signal S is tied low in stage 2. As a result, stage 2 operates as a synchronous divide-by-4, as is shown in Fig. 3. The 8-phase fafc signal with 45° phase difference for multi-phase sampling algorithm is connected from the differential output of Dlatch1∼Dlatch4’s in stage 2 (Q+s and Q−s with blue color in Fig. 3). An M of 16 (2 × 2 × 4) is achieved through the above settings. As a result, fafc is no more than 775 MHz, which is an available clock frequency for RTL realization in 65 nm CMOS design.

Besides the 8-phase clock generation function, a more important reason of using this dual divider is reducing power and area, especially the area cost of stage 0. Although TSPC logic can be used in stage 1, stage 0 can only be designed by CML latches due to its high operation frequency, which is power and area costly, as shown in Fig. 4 and Table I.

Fig. 4 shows the layout of the proposed divider and each stage is labeled and marked with different colors. Table I listed the area and current consumption of each stage, in which the CML divider (stage 0) is the most power hungry and area costly building block.

The dual-mode frequency divider saves the area cost and power consumption of a multi-phase clock generator which should include stage 0∼2 to generate high frequency fafc. The total area of stage 0∼2 is 3540 μm² (which is 1/3 of AFC circuit, more than a half of the proposed divider) and its power consumption is 5.8 mW, both calculated from Table I. The NAND gate S of stage 2 is the only additional circuit (in the dark blue ellipse of Fig. 3) added to the N mode multi-stage divider. Simulation shows that the current consumption of stage 2 is 254 μA with the NAND gate and 232 μA without. The 22 μA current difference is
negligible compared to total power consumption (5 mA) of the divider, which
demonstrates the power efficiency of the proposed divider. The proposed dual-
mode frequency divider embeds multi-stage high frequency clock generation
function in its M mode without increasing circuit and power cost.

4 Simulations results

Defining \( \Delta f \) as the frequency difference between the center of two adjacent tuning
curves, \( f_{\text{resolution}} \) should be less than \( \Delta f/2 \) to distinguish adjacent tuning curves [3].
In this design, PLL output frequency range is 9.14 GHz~12.47 GHz and VCO
simulation shows the desired \( f_{\text{resolution}} \) increases from 16.5 MHz to 40 MHz as
frequency increases. The reason of different \( f_{\text{resolution}} \) between high frequency and low
frequency is because the non-linear relation ship of capacitor value and frequency
[9]. By calculation following equation (1), calibration time of \( 4T_{\text{ref}} \) is needed for
9.5 GHz and \( 2T_{\text{ref}} \) is needed for 12 GHz.

The total AFC time is composed as follows: \( T_{\text{ref}} \) for synchronizing \( f_{\text{ref}} \) and \( f_{\text{afc}} \)
before each comparison, \( kT_{\text{ref}} \) for counting in each comparison step (\( k = 2\sim4 \),
decided by desired \( f_{\text{resolution}} \)), \( T_{\text{ref}} \) for calculation after counting of each step.
Initialization and final code selection processes are finished during several \( T_{\text{afc}} \)
periods and the time cost is negligible compared to \( T_{\text{ref}} \). As a result, time cost of
each bit is \( 3T_{\text{ref}} \) and the total AFC time is counted as \( 6(k + 2)T_{\text{ref}} \) since 6 bit binary

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**Table I.** Area and current consumption of each divider stage

<table>
<thead>
<tr>
<th>Stage</th>
<th>Area (( \mu m^2 ))</th>
<th>Current consumption</th>
<th>Implementation</th>
<th>Stage in M Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stage 0</td>
<td>50*60</td>
<td>3.9 mA</td>
<td>CML</td>
<td>Active</td>
</tr>
<tr>
<td>Stage 1</td>
<td>20*17</td>
<td>646 ( \mu A )</td>
<td>TSPC</td>
<td>Active</td>
</tr>
<tr>
<td>Stage 2</td>
<td>20*10</td>
<td>254 ( \mu A )</td>
<td>TSPC</td>
<td>Active</td>
</tr>
<tr>
<td>Stage 3~7</td>
<td>50*20</td>
<td>215 ( \mu A )</td>
<td>RTL</td>
<td>Bypassed</td>
</tr>
<tr>
<td>Total</td>
<td>50*100</td>
<td>5 mA</td>
<td>/</td>
<td>Switching connection</td>
</tr>
</tbody>
</table>

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**Fig. 4.** Layout of the proposed dual-mode divider
capacitor bank is adopted, which is 0.96 µs (k = 2) and 1.44 µs (k = 4) for high and low target frequencies, respectively.

VCO frequency range of this design is 9.14 GHz–12.47 GHz, covered by 64 tuning curves, and the distance between center spots (V_{tune} = 0.6 V) of two adjacent tuning curves increases from 33 MHz to 80 MHz (Δf) as frequency increases, in correspondence with the required 16.5 MHz and 40 MHz f_{resolution}.

12 GHz and 9.5 GHz are taken as the desired frequency for large f_{resolution} and small f_{resolution} for transient simulation, respectively, to demonstrate the correctness and precision of the proposed AFC circuit.

Fig. 5 shows VCO frequency (and their corresponding V_{ctrl[5:0]}) variation during AFC process for 12 GHz target frequency. Comparison period is set to 4T_{ref}, 2T_{ref}, 1T_{ref} in Fig. 4(a), (b), (c), and the corresponding calibration time is 1.44 µs, 0.96 µs and 0.72 µs, respectively. AFC process finishes after 6-steps comparison

![Fig. 5. VCO frequency and capacitor bank control bits variation during AFC process (The target frequency is 12 GHz)](image)

Fig. 6. Frequency and V_{tune} variation during loop settling transient (The target frequency is 12 GHz)
and all three calibration process shown the same frequency searching route in Fig. 5(a), (b) and (c), which demonstrate the comparison time of a $T_{\text{ref}}$ (40 ns) achieves correct calibration result for 40 MHz frequency resolution. The 639 mV steady state $V_{\text{tune}}$ voltage shown in Fig. 6 also proves that an accurate calibration result is achieved after a calibration of 0.72 µs, since steady state $V_{\text{tune}}$ voltage is nearby $V_{\text{dd}}/2$ (600 mV for 1.2 V $V_{\text{dd}}$). In addition, 0.72 µs is the shortest achievable AFC time because only one $T_{\text{ref}}$ is used for comparison. Settling time of analog loop is much longer than AFC time (about 10 µs) such that the AFC time is not a major concern of PLL settling time.

For 9.5 GHz target frequency, 4$T_{\text{ref}}$ comparison time is necessary for 33 MHz $f_{\text{resolution}}$ since calibration process experience incorrect step (signed with red color in Fig. 7) for 1$T_{\text{ref}}$ and 2$T_{\text{ref}}$ comparison time, which matches the calculation at the

![Fig. 7. VCO frequency and capacitor bank control bits variation during AFC process (The target frequency is 9.5 GHz)](image)

![Fig. 8. Frequency and $V_{\text{tune}}$ variation during loop settling transient (The target frequency is 9.5 GHz)](image)
start of this section. Although the searching goes back to optimal code after the final code selection period, it is because calibration has reached optimum code 010000 at the second step. Otherwise, an incorrect calibration result might be chosen and the PLL will never reach steady state at all. The 505 mV steady state $V_{\text{tune}}$ is close to $V_{DD}/2$ in Fig. 8, which proves that an optimum final code is selected after 1.44 µs calibration.

<table>
<thead>
<tr>
<th>Table II. Performance summary and comparison</th>
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<tbody>
<tr>
<td>AFC scheme</td>
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<tr>
<td>Search algorithm</td>
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<td></td>
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<tr>
<td>AFC time reduction method</td>
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<tr>
<td>Digital control block</td>
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<tr>
<td>Clock generator</td>
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<tr>
<td>Time to voltage converter</td>
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<tr>
<td>Analog comparator</td>
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<tr>
<td>AFC power consumption</td>
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<tr>
<td>AFC Area (mm²)</td>
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<tr>
<td>Reference frequency (MHz)</td>
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<tr>
<td>Single bit comparison time for a resolution of $f_{\text{ref}}$</td>
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<tr>
<td>Finest resolution achievable in a unit cycle ($T_{\text{ref}}$)</td>
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<tr>
<td>AFC time (µs)</td>
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<tr>
<td>PLL output Frequency (GHz)</td>
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<tr>
<td>Technology</td>
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</table>

*Power consumption of the multi-phase clock generator is not mentioned in [7]. Since divider power is highly related to input frequency, the M-mode (first 3 stages) divider power (5.8 mW) in this design can be used for comparison.

# Multiplied by 4 during AFC transient.
A performance comparison between the proposed AFC technique and published designs [4, 5, 6, 7] is listed in Table II. The proposed AFC achieves the fastest calibration time through the multi-phase sampling algorithm among all counter based AFC techniques [4, 7]. The proposed calibration algorithm achieves the least calibration time for a resolution of $f_{\text{ref}}$ and the finest resolution in a unit reference cycle ($T_{\text{ref}}$), which is better than all mentioned publications. The proposed fast AFC circuit has no power consumption at steady state, which is an important advantage compared to analog AFCs [5, 6]. Area of the proposed AFC is also the smallest compared to mentioned publications, which demonstrated the proposed AFC is the most efficient technique among published fast AFCs.

5 Conclusions

A fast and efficient AFC technique designed for high frequency PLLs is introduced in this article. The proposed AFC circuit utilizes high frequency counters to reduce comparison time and a multi-phase sampling technique is proposed to reduce AFC time while not degrading calibration precision. The proposed AFC is efficient because of the presented dual-mode frequency divider. The frequency divider is used as a multi-phase high frequency clock generator for AFC during calibration process, which saves the circuit cost and power dissipation for high frequency clock generation. The proposed fast and efficient AFC technique achieves very short calibration time, the smallest unit cycle frequency resolution, the least circuit cost and zero power dissipation, which are all competitive among mentioned AFC techniques.