Clover shape layout technique in switched capacitor power amplifier for improving drain efficiency

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Abstract: In this paper, a new layout technique for improving drain efficiency of the switched capacitor power amplifier (SCPA) is proposed. To minimize the line length from the output capacitors to the output, capacitors and amplifiers are placed around the output pad. This reduces parasitic capacitances and resistances of the output line. Simulation result shows 3% improvement in the drain efficiency. The fabricated test chip achieves 24% drain efficiency at 7 dB back-off while delivering 11 dBm output.

Keywords: SCPA, drain efficiency, layout technique, clover shape layout

Classification: Integrated circuits

References

1 Introduction

M2M (Machine To Machine) communication is attracting a research interest as the next generation communication system. A variety of things connected to the system are controlled by using data delivered from wireless sensors. Recently, the IEEE 802.11ah is being developed targeting wireless sensor node, which operates at sub-GHz license-exempt bands to provide improved transmission range as compared to the WLANs at 2.4/5 GHz bands. Besides, in the IEEE 802.11ah, each channel is placed closed to the next channel, resulting the channel placement more crowded than the WLANs.

Since the IEEE 802.11ah employs orthogonal frequency division multiplexing (OFDM) signal which has a large peak-to-average ratio (PAR), it is highly required to develop a power amplifier (PA) that offers excellent efficiency with high linearity.

While using a linear PA with large back-off is a standard choice, the digital power amplifier (DPA) gains considerable interest as a possible alternative [1, 2, 3, 4, 5]. In [4] and [5], Yoo et al. proposed a switched capacitor PA (SCPA) which comprises an array of capacitors that are switched either to the supply voltage or ground at the RF carrier frequency. The SCPA can be viewed as digitally-modulated envelope elimination and restoration (EER) that achieves high average efficiency with superior linearity.

Considering the usage as wireless sensor devices, low power dissipation is one of the most important elements to maximize battery lifetime. Therefore, the SCPA can be considered as a good candidate. However, in actual implementation the drain efficiency is significantly degraded due to parasitic elements, in particular those at the output terminal of the SCPA output.

In this paper, we propose a layout technique to enhance the drain efficiency by minimizing parasitic elements of the SCPA output line.

2 Circuit diagram of SCPA

Fig. 1 shows a simplified circuit diagram of the SCPA. It consists of plural class-D PAs, capacitors $C_s0$ and a resonant inductor $L$. The array of class-D PAs are activated or inactivated based on the AM Code.

Under the ideal condition, output voltage of the SCPA is proportional to the number of active class-D PA determined by AM Code. Hence, output voltage is written as Eq. (1) where $N$ is the bit-width of AM Code and $n$ is the number of activated class-D PAs [4].

$$V_{out} = \frac{2}{\pi} \left( \frac{n}{N} \right) V_{DD}.$$  (1)

In an inactive mode, the gate voltages of both PMOS and NMOS transistors become high, connecting the input of $C_{s0}$ to $V_{SS}$. In an active mode, the square voltage wave form at carrier frequency $f_c$ is applied to both PMOS and NMOS transistors. The drain voltages are switched between power supply voltage $V_{DD}$ and $V_{SS}$, generating a square wave output at $f_c$. The SCPA’s output is filtered by the resonance circuit and matching network, delivering a sine wave output to the 50Ω load.
Even though the SCPA achieves high efficiency, the parasitic elements on the output line degrade drain efficiency. In the next chapter, we analyze the impact of these parasitic elements on the SCPA.

![Fig. 1. Simplified circuit diagram of the SCPA](image)

### 3 Theoretical analysis of drain efficiency for SCPA

Fig. 2 shows the circuit diagram of the SCPA including parasitic capacitance and resistance.

![Fig. 2. Circuit diagram of SCPA with parasitic capacitance and resistance](image)

In Fig. 2, $C_p$ represents the total parasitic capacitance of the output lines which connect output capacitors to the output pad. $R_{on}$ is the ON resistance of the final stage transistors. $R_l$ is the total equivalent resistance of the wirings. $C_x$ is the total capacitance of the output capacitors. $C_d$ is the total parasitic capacitance of all the output transistors. $C_t$ is the total parasitic capacitance of the wirings which connects the amplifier to the output capacitor.

To have better understanding of the analysis, we start with the simplified equivalent circuit shown in Fig. 3 where parasitic capacitance is ignored. In Fig. 3, $R_{load}$ is the load impedance looked into the matching network from the SCPA and $R_p$ is the total of the parasitic resistance of the wirings as well as output transistor ON resistance, bonding wire of the SCPA output and the resonant inductor $L$. $V_1$ is the peak-to-peak voltage applied to $R_p + R_{load}$. $N$ is the total number of capacitors $C_{s0}$, and $n$ is the number of capacitors $C_{s0}$ whose bottom plates are switched between $V_{DD}$ and $V_{SS}$. 
The output power $P_{\text{out}}$ (the power supplied to the total resistance $R_p + R_{\text{load}}$) and $P_{\text{load}}$ (the power supplied to $R_{\text{load}}$) are given by the following equations [4].

\[
P_{\text{out}} = \frac{2}{\pi^2} \frac{V_1^2}{R_p + R_{\text{load}}} = \frac{2}{\pi^2} \frac{1}{(R_p + R_{\text{load}})^2} \left(\frac{n}{N}\right)^2 V_{DD}^2 \quad (2)
\]

\[
P_{\text{load}} = P_{\text{out}} \times \frac{R_{\text{load}}}{R_p + R_{\text{load}}} = \frac{2}{\pi^2} \frac{R_{\text{load}}}{(R_p + R_{\text{load}})^2} \left(\frac{n}{N}\right)^2 V_{DD}^2. \quad (3)
\]

Assuming that the switching operation of the capacitors is ideal, the dynamic power required for charging and discharging the capacitor array is expressed as

\[
P_{\text{SC}} = C_{\text{in}} V_{DD}^2 f, \quad (4)
\]

where $C_{\text{in}}$ is the total capacitance seen from power supply.

Since $C_s$ and $L$ form the loss-less resonant circuit, the total power $P_{dc}$ (the total power consumption of the SCPA) is equal to the sum of $P_{\text{out}}$ and $P_{\text{SC}}$. Then the drain efficiency $\eta$ is derived as

\[
\eta = \frac{P_{\text{load}}}{P_{\text{out}} + P_{\text{SC}}}. \quad (5)
\]

Next, considering the parasitic capacitances $C_p$, $C_i$ and $C_d$, the equivalent circuit is modified as Fig. 4. This can be further simplified to Thevenin equivalent circuit shown in Fig. 5.
Based on Fig. 5, the peak-to-peak voltage applied to $R_p + R_{load}$ is calculated as

$$V_1 = \frac{n}{N} \frac{C_s}{C_s + C_p} V_{DD}.$$  \hfill (6)

Substituting Eq. (6) into (2), $P_{out}$ is given by

$$P_{out} = \frac{2}{\pi^2} \frac{n}{N} \left( \frac{C_s}{C_s + C_p} \right)^2 \frac{V_{DD}^2}{R_p + R_{load}}.$$  \hfill (7)

Then, the power supplied to the load resistance is calculated as follows.

$$P_{load} = \frac{2}{\pi^2} \frac{R_{load}}{(R_p + R_{load})^2} \left( \frac{n}{N} \right)^2 \left( \frac{C_s}{C_s + C_p} \right)^2 V_{DD}^2.$$  \hfill (8)

To calculate the capacitance seen from the power supply, we use the equivalent circuit shown in Fig. 6.

![Fig. 6. Total capacitance looked from power line](image)

From Fig. 6, the total capacitance $C_{in}$ is given as

$$C_{in} = \frac{n}{N} \left( C_d + C_l \right) + \frac{n(N - n)C_s^2 + nNC_sC_p}{N^2(C_s + C_p)}.$$  \hfill (9)

Substituting Eq. (4), (7), (8) and (9) into (5), the drain efficiency $\eta$ is calculated as follows.

$$\eta = \frac{4n^2C_s^2}{4n^2C_s^2 + 2\pi^2f(C_s + C_p)(R_p + R_{load})[n(N - n)C_s^2 + nN(C_sC_p + (C_s + C_p)(C_d + C_l))] \times \frac{R_{load}}{R_p + R_{load}}}.$$  \hfill (10)

For simplification, we assume $R_p$ is constant regardless of $n$, which is given by

$$R_p = R_{on} + R_l + R_{WL}.$$  \hfill (11)

where $R_{WL}$ is the total resistance of the bonding wire and the resonant inductor $L$. From Eq. (8), (10) and (11), $P_{load}$ and $\eta$ of the SCPA are expressed as follows.

$$P_{load} = \frac{2}{\pi^2} \frac{R_{load}}{(R_{on} + R_l + R_{WL} + R_{load})^2} \left( \frac{n}{N} \right)^2 \left( \frac{C_s}{C_s + C_p} \right)^2 V_{DD}^2.$$  \hfill (12)

$$\eta = \frac{4n^2C_s^2}{4n^2C_s^2 + 2\pi^2f(C_s + C_p)(R_{on} + R_l + R_{WL} + R_{load})[n(N - n)C_s^2 + nN(C_sC_p + (C_s + C_p)(C_d + C_l))] \times \frac{R_{load}}{(R_{on} + R_l + R_{WL} + R_{load})}}.$$  \hfill (13)
Based on Eq. (12) and (13), $C_P$ adversely affects $P_{load}$ and $\eta$ because it determines the ratio between the power generated by the PA and the power delivered to the load. On the other hand, $C_d$ and $C_l$ affect only $\eta$. This is because charge and discharge currents are increased by $C_d$ and $C_l$, but they do not change the voltage swing at the output node. From these observations, it is understood that reducing $C_P$ is effective to improve both $P_{load}$ and $\eta$.

4 Clover shape layout technique

In conventional DPA layout, output transistors are placed close to each other in straight line to minimize process variation [6]. In the SCPA, capacitors and amplifiers are also placed in the same way.

Fig. 7 shows the typical SCPA layout which we name “rectangular shape layout”. Each unit is composed of identical capacitors and amplifiers which are placed in the straight line. The output lines from each output capacitor to the output pad are connected by shortest route. In this layout, the output line length between the output pad to the output capacitors depends on the placement of capacitors. For example, center capacitors connected to the output pad achieves shortest line length. But the capacitors are placed far away from the output pad, requiring long length routing. This results in larger parasitic capacitance, degrading drain efficiency.

![Fig. 7. Typical SCPA layout (rectangular shape layout)](image1)

Because $C_P$ affects both $P_{load}$ and $\eta$, series capacitors $C_{s0}$ need to be placed close to the output pad to minimize $C_P$. To satisfy this requirement, we propose a “clover layout” shown in Fig. 8. In this layout, series capacitors $C_{s0}$ are placed on the concentric circle, and the output pad is placed at a center. In addition, amplifiers are placed on the outer concentric circle next to the inside one.

![Fig. 8. Proposed SCPA layout (clover shape layout)](image2)
By using this technique, each signal routing from the output pad to the capacitor and the amplifier is minimized.

5 Simulation and measurement results

A test chip of the SCPA employing proposed clover layout is fabricated in 40 nm CMOS technology. In the typical layout (Fig. 7), the minimum length from a series capacitor to the output pad is 120 µm and the maximum length is 980 µm. In the proposed layout (Fig. 8), the minimum length is 105 µm and the maximum length is 350 µm which is about one–third of the conventional approach.

Fig. 9 shows the simulation results of the proposed SCPA. In this figure, green lines represent power and drain efficiency estimated by Eq. (12) and (13). The power supply voltage ($V_{DD}$) is 2.75 V and the carrier frequency ($f_c$) is 920 MHz. In this simulation, parasitic elements were extracted using layout parasitic extraction (LPE) in order to consider the influence of parasitic capacitance and resistance of the output wiring. Parameters are listed in Table I.

![Fig. 9. Simulation and analysis results of (a) $P_{load}$, (b) $\eta$](image)

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If we compare the drain efficiencies at 7 dB back-off, which are indicated by arrows in Fig. 9(a), the proposed clover shape layout achieves 30% efficiency with 12.1 dBm output. On the other hand, the typical rectangular layout gives 27% with
11.6 dBm. Thus, the proposed technique offers 3% improvement in the drain efficiency. Even though the drain efficiency of the clover shape layout becomes lower at higher AM code due to the large $C_l$, this is not critical in terms of the modulated efficiency because of the large PAR of the OFDM modulation.

Fig. 10 shows the measurement results. Carrier signal is provided from a PLL circuit which is fabricated on the same die. The measured drain efficiency at 7 dB back-off ($P_{load} = 11$ dBm) is 24% which is 6% lower than the simulated result. This will be attributed to unaccounted parasitics, but further study is required to locate sources of degradations.

![Fig. 10. Measurement results of (a) $P_{load}$, (b) $\eta$](image)

6 Conclusion

In this work, we have proposed a SCPA layout technique that improves drain efficiency. Using this technique, output capacitors and the output pad can be connected by shortest route, minimizing parasitic capacitance and resistance. Simulation results show 3% improvement of the drain efficiency. The fabricated chip achieves 24% drain efficiency at 7 dB back-off while delivering 11 dBm output.

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