A compact programmable LDO regulator for ultra-low voltage SoC

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Abstract: This paper proposes a compact programmable low dropout (LDO) regulator for an ultra-low voltage system-on-a-chip (SoC) using the voltage scaling technique. Two innovative design concepts were proposed: a programmable multi-level resistor array that can precisely tune the ratio of the feedback resistor divider; and a current limiter that limits a small static current flowing through the resistor network while reducing the occupied area. Experimental results show that the monotonic 50-step programmable output ranging from 0.3 V to 0.8 V is achieved, with an input of 1 V and a maximum load current of 100 mA. The occupied area is only 0.017 mm\textsuperscript{2}.

Keywords: LDO, programmable, voltage scaling

Classification: Integrated circuits

References


1 Introduction

The power management unit (PMU) has been widely adopted by many energy-restricted, low-voltage (LV) SoC that implement voltage scaling technique to save power. Such a PMU usually uses a main switching converter to achieve high
conversion efficiency (> 90%) for a large voltage conversion range, while several programmable LDO regulators suppress the ripple noise and generate tunable outputs. Several previous studies have focused on designing a programmable LDO regulator [1, 2, 3, 4, 5, 6]. A complex programmable voltage reference and an error amplifier (EA) with a wide input common mode range are required in [1, 2, 3]; the area and power consumption also increase accordingly (e.g. a voltage-to-current converting circuit and a 32-switches array are used in [1] to provide a reference voltage with 80 mV tuning resolution). In [4, 5], a complex switch array (one switch plus one resistor for one tuning step) is required to adjust the resistance value of the feedback network; only a few tuning steps (e.g. the 4-step in [4]) are available to reduce the efficiency of the voltage scaling. More recently, in [6], a 32-step output was achieved by using a current digital-to-analog converter and a current summing circuit to adjust the feedback voltage accordingly. Extra circuit consumes quiescent current and area, while two ideal reference voltages reduce the practicality.

In this paper, we propose a compact, high tuning resolution LV LDO regulator with a programmable multi-level resistor array (PMRA), a current limiter, and a LV bandgap reference (BGR) to provide a monotonic 50-step programmable output ranging from 0.3 V to 0.8 V.

Fig. 1. Design concepts and a practical example of the proposed PMRA and current limiter.

2 The design concepts of PMRA and current limiter

In the LDO regulator shown in upper left Fig. 1, the feedback voltage ($V_{FB}$) approaches the reference voltage ($V_{REF}$) because a high gain EA results in a sufficient high loop gain. Therefore, the relationship between output ($V_{OUT}$) and $V_{REF}$ can be expressed as

$$V_{OUT} = V_{REF} + (R_1/R_2) \times V_{REF},$$  \hspace{1cm} (1)
where two resistors $R_1$ and $R_2$ form the feedback network. In Eq. (1), the lowest voltage level of $V_{OUT}$ is $V_{REF}$ and we can tune the value of $R_1/R_2$ to adjust $V_{OUT}$. The overall tuning range ($V_{range}$) is therefore defined as $(V_{OUT,\text{max}} - V_{REF})$ where $V_{OUT,\text{max}}$ represents the maximum output voltage of the LDO regulator, which must be less than the input voltage ($V_{DD}$). Previous studies use switches to connect resistors in series [4] or in parallel [5] and as a result, each voltage-tuning step requires one switch and one resistor. To satisfy an $m$ voltage tuning steps requirement, the design complexity of these conventional programmable resistor networks [4, 5] is of the order $O(2^m)$, which limits the programmability. In this paper, we propose a PMRA, as the concepts shown in lower left Fig. 1, to reduce the design complexity to the order of $O\left(\frac{2^n}{C_{2\sqrt{mn}}+n}\right)$, where $n$ represents the level number. To explain the principles of the proposed PMRA, we define some parameters as follows: $V_{res,L}$, $R_{Li}$, and $N_{Li}$ represent the voltage tuning resolution, resistance value, and number of resistors for each hierarchical level $i$, respectively. $a_i$ represents the ratio of tuning resolution between level $i$ and level $(i+1)$. Eq. (2) expresses the relationship between these parameters.

$$\begin{align*}
a_i = & \begin{cases} V_{res,L,(i+1)}/V_{res,L,i}, & i = 1 \sim (n-1) \\ V_{range}/V_{res,L,i}, & i = n \end{cases} \\
R_{Li} = & (V_{res,L,i}/V_{REF}) \times R_2, & i = 1 \sim n \\
N_{Li} = & \begin{cases} a_i, & i = 1 \\ a_i - 1, & i = 2 \sim n \end{cases}
\end{align*}$$

Then we take the practical case in right Fig. 1 as an example, to describe how we obtain $R_{Li}$ and $N_{Li}$ for our proposed PMRA for a specified $V_{REF}$, $V_{range}$, $V_{res,L1}$, and selected $n$. This example shows the design of an LDO regulator with $V_{OUT}$ equal to 0.3 V–0.9 V and a voltage tuning resolution of 5 mV ($V_{res,L1}$); the $V_{REF}$ and $V_{range}$ are specified as 0.3 V and 0.6 V. When $n$ and $V_{res,L2}$ are selected to be 2 and 100 mV, we can use (2) to derive $\{R_{L1,1}, R_{L2}\} = \{R_2/60, R_2/3\}$ and $\{N_{L1,1}, N_{L2}\} = \{20, 5\}$. The total number of resistors is 25 and the number of switches is 27, as two extra switches are required to bypass all resistors. When $n$ and $\{V_{res,L2}, V_{res,L3}\}$ are selected to be 3 and $\{50 \text{ mV, } 300 \text{ mV}\}$ respectively, we use (2) to derive $\{R_{L1,1}, R_{L2}, R_{L3}\} = \{R_2/60, R_2/6, R_2\}$ and $\{N_{L1,1}, N_{L2}, N_{L3}\} = \{10, 5, 1\}$. Therefore, the total number of resistors and switches is reduced to 16 and 19, which reduces the design complexity. The above example shows that our proposed 3-Level PMRA can effectively reduce the total number of resistors/switches required from 120/121 to 16/19 while satisfying the 120-voltage tuning step requirement.

The value of $R_2$ will determine the static current flowing through the feedback resistor network ($I_{R_2}$), which can be expressed as Eq. (3). As this static current decreases the current efficiency of the LDO regulator, we may select $R_2$ equal to multi-KΩ, which occupies a considerable area. We further propose a current limiter by replacing $R_2$ with a constant current source, which can be a simple n-type MOS transistor biasing in the saturation region, as the example shown in lower right Fig. 1. As a result, Eq. (1) is modified to be Eq. (4), where $R_1$ is still designed by the PMRA described above.
\[ I_{RQ} = \frac{V_{REF}}{R_2} \]  
\[ V_{OUT} = V_{REF} + I_{RQ} \times R_1 \]

3 Circuit implementations

A LV programmable LDO regulator was designed to show the efficiency of the proposed PMRA and current limiter, of which the complete circuitry is illustrated in Fig. 2. To enable operation at a supply voltage of sub-1-V, we employ a high gain current-split operational transconductance amplifier (OTA) \([7]\) composed of \(M_1\)–\(M_{11}\) as the EA. The p-type input differential pair (\(M_1\)–\(M_2\)) is selected to support a lowest output level of 0.3 V (i.e. \(V_{FB}\) and \(V_{REF}\) can be as low as 0.3 V), while the output stage composed of \(M_8\)–\(M_{11}\) provides a nearly rail-to-rail signal swing to drive the power MOS transistor (\(M_P\)) and minimize the transistor size. And we can keep the non-dominant pole \(p_g\) far away from the dominant pole \(p_O\) for an off-chip compensated LDO regulator. As a result, it is easy to create the pole-zero cancellation (\(p_O\) and \(z_{esr}\)) and achieve a stable operation over a wide output tuning range. Further a low-voltage BGR is adapted from \([8]\) by modifying the active load to provide a \(V_{REF}\) of 0.3 V, and satisfies the minimum \(V_{OUT}\) requirement of 0.3 V. To provide an output voltage range of 0.3 V–0.8 V (\(V_{range} = 0.5\) V) with a tuning resolution of 10 mV (\(V_{res,1}\)), we chose a 2-level resistor array architecture (\(n = 2\)) and define a 100 mV tuning resolution for the 2nd level resistor array (\(V_{res,2}\)). We also apply the current limiter (\(M_{limit}\)) to limit \(I_{RQ}\) to 10 µA. The current limiter is biased by the pre-existing bias voltage (\(V_{B2}\)) which will never increase the complexity of biasing circuitry. From Eq. (2) and Eq. (3), we can derive the resistance values (\(R_{L1}, R_{L2}\)) and number (\(N_{L1}, N_{L2}\)) for the first and second level resistor arrays as \(\{1 \, \text{K} \Omega, 10 \, \text{K} \Omega\}\) and \(\{10, 4\}\). The switches are implemented using transmission gates to ensure a wide output voltage range. Note that it reduces the total number of resistors/switches required from \(50/51\) to \(14/16\) and confirms the design complexity reduction from \(O(2m)\) to \(O(2n \times \sqrt{m} + n)\) with \(m, n = \{50, 2\}\).
4 Experimental results

The proposed programmable LDO regulator (Fig. 2) was fabricated using the 1-V TSMC 90 nm CMOS process technology, and Fig. 3(a) and (b) shows the die micrograph and layout, respectively. Fig. 4(a) illustrates the measured output voltage with 10 mV tuning resolution for a 0.3 V–0.8 V tuning range, which shows very good monotony. The load transient variations were also verified to show the loop response and stability. Fig. 4(b) shows that the output variation (ΔV_{OUT}) is only 18 mV for a 0.1 mA–100 mA load current transient at V_{DD}/V_{OUT} = 1 V/0.3 V, which shows an accurate output. Fig. 4(c) shows the line regulation of 12.4 mV/V at V_{DD} = 0.75 V–1.8 V and I_{OUT}/V_{OUT} = 5 mA/0.3 V while Fig. 4(d) shows the load regulation of 0.18 mV/mA at I_{OUT} = 0.1–100 mA and V_{DD}/V_{OUT} = 1 V/0.3 V. Table I summarizes the experimental results and shows that

![Image](image-url)

**Fig. 3.** (a) Die micrograph and (b) layout of the proposed low-voltage programmable LDO regulator.

![Image](image-url)

**Fig. 4.** Measurement results: (a) 50 steps programmable output voltage, (b) output variations during load transient test, (c) line regulation, and (d) load regulation.
our proposed LDO regulator with PMRA and current limiter provides more tuning steps than all previous designs, and accurately adjusts the output voltage with a resolution of 10 mV. Even with the inclusion of the bandgap reference circuit, the proposed LDO regulator still shows efficiency in terms of quiescent current and occupied area.

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Technology (CMOS)</td>
<td>0.18 µm</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>0.18 µm</td>
<td>90 nm</td>
</tr>
<tr>
<td>(V_{DD}) (V)</td>
<td>1.8</td>
<td>3.3–1.2</td>
<td>4.2</td>
<td>3.3</td>
<td>1.6</td>
<td>1.8–0.75</td>
</tr>
<tr>
<td>(V_{OUT}) (V)</td>
<td>1.7–0.9</td>
<td>3.1–1.0</td>
<td>3.3/2.5/1.8</td>
<td>2.8/1.3</td>
<td>1.2–1</td>
<td>0.8–0.3</td>
</tr>
<tr>
<td>Tuning Step/Resolution</td>
<td>N.A.</td>
<td>N.A.</td>
<td>4/800 mV</td>
<td>2/1500 mV</td>
<td>32/6.25 mV</td>
<td>50/10 mV</td>
</tr>
<tr>
<td>Load Capacitor (C_L)</td>
<td>500 pF</td>
<td>0</td>
<td>N.A.</td>
<td>5 µF</td>
<td>100 pF</td>
<td>1 µF</td>
</tr>
<tr>
<td>Max. (I_Q) (µA)</td>
<td>1060**</td>
<td>&gt; 42**</td>
<td>170°</td>
<td>53</td>
<td>120</td>
<td>67*</td>
</tr>
<tr>
<td>Max. (I_{OUT}) (mA)</td>
<td>20</td>
<td>100</td>
<td>100</td>
<td>140</td>
<td>5</td>
<td>100</td>
</tr>
<tr>
<td>Current Efficiency</td>
<td>94.7%**</td>
<td>&lt;99.96%**</td>
<td>99.96%</td>
<td>99.96%</td>
<td>97.6%</td>
<td>99.93%*</td>
</tr>
<tr>
<td>Line Regulation (mV/V)</td>
<td>6</td>
<td>&lt; 1.7%</td>
<td>N.A.</td>
<td>N.A.</td>
<td>9.1</td>
<td>12.4</td>
</tr>
<tr>
<td>Load Regulation (mV/mA)</td>
<td>0.5</td>
<td>&lt; 1.5%</td>
<td>N.A.</td>
<td>N.A.</td>
<td>0.122</td>
<td>0.18</td>
</tr>
<tr>
<td>Output Variation (\Delta V_{OUT}) @((I_{OUT1}-I_{OUT2})) in mA</td>
<td>&gt;300 mV</td>
<td>&lt;90 mV</td>
<td>98 mV</td>
<td>&gt;120 mV</td>
<td>370 mV</td>
<td>18 mV</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.006**</td>
<td>0.35**</td>
<td>0.28°</td>
<td>N.A.</td>
<td>0.16</td>
<td>0.017*</td>
</tr>
</tbody>
</table>

*With including the BGR **Without including the programmable BGR

5 Conclusion

The proposed programmable LDO regulator is suitable for adaptive \(V_{DD}\), ultra-low voltage SoC to save power. It uses a regular programmable multi-level resistor array with a current limiter to efficiently generate a monotonic 50-step programmable output ranging from 0.3 V to 0.8 V, with a maximum load current of 100 mA. The occupied area is only 0.017 mm².

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