Multiple nodes upset tolerance DICE latch based on on-state transistor

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Abstract: A reliable single-event upset (SEU) hardened latch is proposed to enhance the multiple nodes upset tolerance. By using the on-state transistor, half of the sensitive transistor pairs can be reduced compared to the typical DICE latch. Technology computer-aided design (TCAD) simulation is used to verify the hardening performance of our proposed latch.

Keywords: multiple nodes, DICE, on-state transistor, SEU

Classification: Integrated circuits

References

1 Introduction

Space radiation induced soft errors are becoming a great threat to integrated circuits (ICs). If the data in latches is changed due to the ions radiation, this is referred to a single event upset (SEU). Previous research has illustrated that the vulnerability of latches to SEU is increasing with technology scaling [1].

At present, lots of redundancy based latches are proposed to mitigate the SEU [2, 3, 4]. These latches are effective to eliminate the SEU when only one node collects charge. Whereas, when two or more nodes collect charge simultaneously, the hardening performance is invalid. Charge sharing is becoming serious in advanced technologies [5, 6, 7, 8]. This is a great challenge for the redundancy based latch [9, 10, 11].

Several layout-level approaches are presented to reduce the multi-node charge collection [12, 13]. These layout-level approaches are difficult to be applied to the standard cells as the layout height of the latches is changed. In this paper, a reliable SEU hardened latch based on the on-state transistor is designed. The TCAD simulations are conducted to evaluate the multiple nodes upset tolerance of this hardened latch.

2 Challenges for traditional redundancy based hardened latches

At present, lots of redundancy based hardened latches, such as DICE, QUATRO and DMR, are designed to mitigate SEU [2, 3, 4]. These hardened latches have proved to be effective RHBD latches when only one node collects charge [2]. However, multiple nodes charge collection will attenuate the hardening performance of these latches [7, 9].

![Typical DICE latch](image)

The DICE latch is a typical hardened latch based on redundancy to mitigate SEU [2]. As presented in Fig. 1. The state value of each node is controlled by two
adjacent nodes. By doing this, the state change on any node will not result in an upset due to the other three unchanged nodes. In this paper, the DICE redundancy structure not the clock and data input part is studied.

The sensitive transistor pairs are defined as any two transistors which can cause an upset when they collect charge concurrently [5]. The SPICE simulation is carried out to identify the sensitive transistor pairs in the DICE latch. During the simulation, the output nodes of any combination of two transistors in the DICE structure are injected with charge. And the output of node QN is monitored to judge whether an upset occurs. Table I presents the sensitive transistor pairs in the DICE structure with different state values.

Table I. Sensitive transistor pairs in the DICE structure

<table>
<thead>
<tr>
<th>State Value of Node n1, n2, n3, n4</th>
<th>0101</th>
<th>1010</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sensitive Transistor Pairs</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(P1, P3) (N2,N4)</td>
<td></td>
<td>(P2, P4) (N1,N3)</td>
</tr>
<tr>
<td>(P1, N2) (P1,N4)</td>
<td></td>
<td>(P2, N1) (P2,N3)</td>
</tr>
<tr>
<td>(P3, N2) (P3,N4)</td>
<td></td>
<td>(P4, N1) (P4,N3)</td>
</tr>
</tbody>
</table>

The decreased distance between these sensitive transistor pairs has made this DICE structure more vulnerable to multi-node charge collection [6]. Related work has pointed out that the performance of DICE to mitigate SEU was largely decreased due to charge sharing [9, 14]. Other redundancy based latches also face this challenge [3, 4]. To enhance the multiple nodes upset tolerance in latches is becoming important in advanced technologies.

3 On-state transistor

As know, inverters are the essential component of the typical latches. As presented in Fig. 2, this is a dual port hardened inverter proposed in patent [15]. Two on-state transistors are used in this structure. And this inverter can eliminate the single event transient (SET).

![Fig. 2. The dual port hardened inverter presented in [15]](image)

To analyze the SET property of this inverter, TCAD simulations are conducted. Fig. 3 presents the structure for the P-hit analysis. A five-stage inverter chain is designed as the simulation structure. The studied inverter is in the second stage.
An additional NMOS transistor is appended into the traditional inverters. The output node Y is at the cross of these two NMOS transistors. We model the PMOS transistor in the second stage inverter as the three-dimensional numerical model, and the other transistors are modeled as the SPICE model. The three-dimensional numerical models are calibrated to the 65 nm CMOS process compact models.

For this simulation, the input of the inverter chain is “0”. The drain of transistor P1 is struck by ions. Fig. 4 presents the simulation results. We plot the voltage pulse waveform at node X, node n1 and node n2 as the LET of incident ions is 10 MeV·cm²/mg. Although the voltage amplitude at node X is higher than VDD/2, the voltage amplitude at node n1 is only about 0.2 V due to the voltage drop between transistor N2 and transistor N1. The voltage transient at node n1 results in little effect on the next stage inverter. The voltage at node n2 remains to be 1.0v.

![Three-dimensional TCAD model](image)

**Fig. 3.** A five stage inverter chain used to study the P-hit immune inverter

![Voltage waveform](image)

**Fig. 4.** Voltage waveform at node X, n1 and n2 as the LET of ions is 10 MeV·cm²/mg

Similar simulations can also be conducted to verify the hardening performance of this inverter to eliminate the N-hit SET pulse.
4 Proposed SEU hardened latch

4.1 Circuit structure

Fig. 5 presents the structure of our proposed SEU hardened latch. The on-state transistors marked in red color are appended based on the DICE latch. These appended transistors will play the same role as the appended transistors in the inverter shown in Fig. 2.

4.2 Cost performance

We implement this hardened latch by using the 65 nm commercial CMOS process at a supply voltage of 1.0 V. To have a comparison, the typical DICE latch is also implemented. And we compare these two latches in terms of area, propagation delay and power.

The propagation delay is measured by calculating the delay from the input D to output QN as the latch is transparent. To estimate the power consumption, the data activity is set to 100%. That is a new data will be written for every clock cycle. The clock frequency is 200 MHZ.

The simulation results presented in Table II illustrates that the performance of this proposed latch is reduced compared to the typical DICE latch.

<table>
<thead>
<tr>
<th></th>
<th>DICE</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>1</td>
<td>1.25</td>
</tr>
<tr>
<td>Delay</td>
<td>1</td>
<td>1.29</td>
</tr>
<tr>
<td>Power</td>
<td>1</td>
<td>1.24</td>
</tr>
</tbody>
</table>

5 Multiple nodes upset tolerance

5.1 Performance to mitigate multiple nodes upset

According to the property of the on-state transistor, it can be concluded that charge collection on transistor pairs (N1, N3), (P1, P3), (P1, N4), (P2, N1), (P3, N2) and (P4, N3) will not cause an upset in our proposed hardened latch. And half of sensitive transistor pairs are reduced in this latch compared to the typical DICE latch as presented in Table III. TCAD numerical simulation is used to evaluate the multiple nodes upset tolerance of this proposed latch.
A. Charge collection on PMOS-PMOS transistors

Fig. 6 presents the device model. The state value of nodes n1, n2, n3 and n4 is set to 0101. The transistor P1 and P3 presented in Fig. 1 and in Fig. 5 are modeled as three-dimensional numerical model, and the other transistors are modeled as the 65 nm SPICE model. The distance between transistor P1 and P3 is small enough to make these two transistors collect charge concurrently due to a single ion hit. For this simulation, the ions with a LET of 30 MeV·cm²/mg will hit the drain center of transistor P1 normally. The ion strike time is at 500 ps.

<table>
<thead>
<tr>
<th>State Value of Node n1, n2, n3, n4</th>
<th>0101</th>
<th>1010</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Proposed Latch</strong></td>
<td>(N2, N4) (P1, N2) (P3, N4)</td>
<td>(P2, P4) (P2, N3) (P4, N1)</td>
</tr>
<tr>
<td><strong>DICE Latch</strong></td>
<td>(P1, P3) (N2, N4) (P1, N4)</td>
<td>(P2, P4) (N1, N3) (P2, N3)</td>
</tr>
<tr>
<td></td>
<td>(P3, N2) (P3, N4)</td>
<td>(P4, N1) (P4, N3)</td>
</tr>
</tbody>
</table>

Table III. Sensitive transistor pairs in the proposed latch and DICE latch

Fig. 6. Device model used to simulate charge collection on transistor P1 and P3

![Device model](image)

**Fig. 6.** Device model used to simulate charge collection on transistor P1 and P3

Fig. 7 presents the circuit response of our proposed hardened latch when charge is collected on transistor P1 and transistor P3.

![Circuit response](image)

**Fig. 7.** Circuit response when charge is collected on transistor P1 and transistor P3

Fig. 7(a) presents the circuit response of our proposed hardened latch when transistor P1 and P3 collect charge. Although the voltage amplitude at node n1 and n3 is larger than 0.5 V, the voltage amplitude at node s1 and s3 is only around 0.2 V due to the voltage drop. This will not result in an upset. And the value of node n1 and n3 will return to LOW. However, as to the traditional DICE latch, charge collection on transistor P1 and P3 will result in an upset as presented in Fig. 7(b).
B. Charge collection on PMOS-NMOS transistors

Fig. 8 presents the device model used to simulate charge collection on NMOS-NMOS transistors as the state value of nodes n1, n2, n3 and n4 is set to 1010. The transistor N1 and N3 presented in Fig. 1 and Fig. 5 are modeled as three-dimensional numerical model, and the other transistors are modeled as the 65 nm SPICE model. As charge sharing is not prominent in NMOS transistors in typical twin-well process, the incident direction of ions with a LET of 30 MeV·cm²/mg would be from transistor N1 to transistor N3 to make transistor N1 and N3 collect charge simultaneously. The ions strike time is at 500 ps.

Fig. 9(a) presents the circuit response of our proposed latch when transistor N1 and N3 collect charge. It is indicated that the voltage amplitude at node n1 and n3 would not be pulled down enough to cause an upset. However, this situation would upset the DICE latch as presented in Fig. 9(b).

C. Charge collection on PMOS-NMOS transistors

Fig. 10 presents the device model used to simulate charge collection on PMOS-NMOS transistors as the state value of nodes n1, n2, n3 and n4 is set to 0101. The transistor P3 and N2 presented in Fig. 1 and Fig. 5 are modeled as three-dimensional numerical model, the other transistors are modeled as the 65 nm SPICE model. To simulate charge collection on transistor P3 and N2, the incident direction of ions with a LET of 30 MeV·cm²/mg would be from transistor P3 to transistor N2. The ion strike time is at 500 ps.
Fig. 11(a) presents the circuit response of our proposed latch when transistor P3 and N2 collect charge. Although the voltage amplitude at node n3 has exceeded 1.0 V and the voltage amplitude at node s2 is under 0.0 V, the amplitude at node s3 and n2 has just a slight change due to the use of on-state transistor. This slight change would not result in an upset. And the voltage of node n2 and n3 would return to the original value. However, the DICE latch would be upset under this situation as illustrated in Fig. 9(b). The case is similar when transistor pairs (P1, N4), (P2, N1) and (P4, N3) collect charge concurrently.

The TCAD simulation demonstrates the well multiple nodes upset tolerance performance in our proposed hardened latch. A more promising advantage of this proposed latch is that the hardening performance is affected little by the ions energy according to the property of the on-state transistor.

5.2 Drawbacks of this proposed SEU hardened latch

The main drawback caused by the appended transistor is the critical charge used to upset this proposed latch is reduced compared to the typical DICE latch as shown in Fig. 12. This figure presents the critical charge of the sensitive transistor pairs (P1, N2) and (N2, N4) when the state value of node n1, n2, n3 and n4 is 0101. One optimistic aspect is that the amount of critical charge in our proposed latch is more or less at the same order as the one in the DICE latch.
6 Conclusion

In this paper, a reliable hardened latch to mitigate SEU based on the DICE structure is proposed. By using the on-state transistor, the multiple nodes upset tolerance is enhanced. Three-dimensional TCAD simulation results present that half of sensitive transistor pairs can be reduced compared to the typical DICE latch.