A low-voltage high PSR LDO regulator with a simple ripple cancellation technique

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Abstract: This paper presents a low-voltage low-dropout voltage (LDO) regulator achieving a high power supply rejection (PSR) performance over a wide frequency range. A simple PSR enhancing circuit (PSRE) establishing a power noise (ripple) cancellation mechanism to avoid power noise passing through the power MOS transistor. A LDO regulator adopting the proposed PSRE was designed using a 1-V 90 nm CMOS process to convert an input of 1.2 V–0.8 V to an output of 0.85 V–0.5 V at a load current range of 0–100 mA. Post-layout simulations show that a PSR is above –57 dB at 1 MHz while the output spike during a 0.1 mA–100 mA load transient test is only 14 mV.

Keywords: LDO, high PSR, low voltage

Classification: Integrated circuits

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1 Introduction

Complex system on chip (SoC) is often equipped with an integrated power management unit, which is frequently composed of one main switching regulator and several linear regulators as post-regulators [1, 2]. A main switching regulator accounts for large voltage difference conversion (e.g. 3.6 V to 1.0 V) to keep high efficiency at the expense of significant voltage ripples in a frequency band of few tens of kilo-hertz to few mega-hertz [3, 4]. Therefore, these linear regulators should have good power supply rejection (PSR) performance to generate ripple-less power sources for noise-sensitive load circuits. Besides, low input voltage linear regulators can minimize dropout voltage so as to maintain power efficiency (i.e. low dropout voltage (LDO) regulator). Many PSR enhancing techniques have been proposed in the past decades, e.g. providing a good isolation path between power source and output [5, 6, 7], or providing a ripple cancellation mechanism [2]. Although cascading two LDO regulators [5] or cascoding power MOS transistors [6, 7] can isolate power source and output well; however, the occupied area and minimum dropout voltage increases accordingly. The ripple cancellation technique proposed in [2] can achieve high PSR over a wide frequency range (up to 10 MHz); however, the complex ripple cancellation circuits are power and area-hungry. Also a high PSR at 10 MHz is unnecessary for a general post-regulator. Reference [8] not only provides a good isolation path but creates a perfect ripple cancellation as well; however, the design complexity grows dramatically. Finally, all these previously mentioned techniques require an input voltage larger than 1 V, which are not suitable for low-voltage SoC applications.

A low-voltage high PSR LDO regulator using a 1-V 90 nm CMOS process technology was proposed in this paper to convert an input of 1.2 V–0.8 V to an output of 0.85 V–0.5 V with a full load current of 100 mA. A low-voltage and high gain OTA-based EA was applied first. A simple PSR enhancing circuit is then proposed to achieve a PSR above –57 dB at 1 MHz. The rest of this paper is organized as follows. Section II illustrates the design concepts and circuit realizations of the proposed low-voltage and high PSR LDO regulator. Performance evaluations are shown in Section III, while we conclude this paper in Section IV.

2 The proposed low-voltage high PSR LDO regulator

A basic LDO regulator is mainly composed of error amplifier (EA), power transistor, feedback network, and output capacitor C_L , as shown in Fig. 1 with removing the PSR enhancing circuit (PSRE) temporarily. Since p-type power MOS transistor is often adopted to minimize the dropout voltage for high conversion efficiency, we can easily establish a ripple cancellation mechanism by replicate the power noise at the gate of power MOS transistor (V_G). To perfectly cancel out the power noise, we propose a PSRE to reject the amplified power noise generated by EA while replicating the entire power noise to V_G . The design concept was shown in Fig. 1.

Fig. 1. Design concept of the proposed high PSR LDO regulator.

An EA with common mode feedback (CMFB), a PSRE, and the biasing circuit comprise the proposed high PSR LDO regulator, as the complete circuits shown in Fig. 2. We apply a simple symmetric OTA as the EA to work properly at low supply voltage (≤ 1 V). We further apply the current splitting technique [9] to boost the gain of the EA for achieving fast transient response and high PSR. Due to the fully differential operation of the OTA-based EA, CMFB circuit is required to guarantee the output common mode voltage level of the EA. Here we apply the continuous-time CMFB circuit [10] to avoid the usage of large capacitors. When the output voltage of the EA (V_{x2} and V_{y2}) becomes lower than the required common mode voltage (V_{CM}), the drain currents of M_{C3} and M_{C5} will increase and lower the control voltage (V_{CMFB}). As a result, M_7 and M_8 were turned more by a smaller V_{CMFB} and recover the voltage level of V_{x2} and V_{y2} . As M_P is a p-type device owing to the low supply voltage and low dropout voltage requirements, we proposed a simple PSRE to replicate the power noise at gate terminal of M_P to cancel out the power noise at its source terminal and achieve a high PSR. First, the small signal model shown in lower Fig. 3 and Eq. (1) demonstrate the common mode rejection ratio (CMRR) analyses of the proposed PSRE, in which $g_{mPi|i=1-5}$, $r_{OPi|i=1-5}$ represent the corresponding transconductance, and output resistance of transistors $M_{PSRi|i=1-5}$ while we also assume ($v_c \approx v_{icm}$), ($r_{OP3} \gg 1/g_{mP1}$), ($g_{mP3} = g_{mP4}$) and ($g_{mP1} \approx g_{mP2}$). Eq. (1) shows that v_g generates a nearly zero output (i.e. good CMRR), as corresponding to the input common mode signal (v_{icm}):

$$\begin{aligned} v_g &= (i_{d2} - i_2) \times r_{OP2} = (g_{mP2} \times v_{g1} - v_{icm}/2r_{OP5}) \times r_{OP2} \\ &\approx \left(g_{mP2} \times \frac{v_{icm}}{2r_{OP5}} \times \frac{1}{g_{mP1}} - \frac{v_{icm}}{2r_{OP5}} \right) \times r_{OP2} \\ &= \left(\frac{g_{mP2}}{g_{mP1}} \times \frac{v_{icm}}{2r_{OP5}} - \frac{v_{icm}}{2r_{OP5}} \right) \times r_{OP2} \approx 0, \end{aligned} \quad (1)$$

Then we ground nodes v_{x2} and v_{y2} and use the small-signal model shown in upper Fig. 3 and Eq. (2) to demonstrate the replication of power noise, where we assume ($r_{OP3} \approx r_{OP4}$). Eq. (2) shows that the proposed PSRE can replicate almost all power noise (v_{dd}) to node v_g in this situation:

$$v_g = v_{dd} \times \frac{r_{OP4}}{r_{OP2} + r_{OP4}} + i_{dd} \times (r_{OP2} \parallel r_{OP4}) \quad (2)$$

$$\approx v_{dd} \times \frac{r_{OP4}}{r_{OP2} + r_{OP4}} + \frac{v_{dd}}{r_{OP3}} \times \left(\frac{r_{OP2} \times r_{OP4}}{r_{OP2} + r_{OP4}} \right) \approx v_{dd},$$

Application of the superposition theorem by summing Eq. (1) and Eq. (2), we see that almost the entire power supply noise is replicated to the gate terminal of M_P (v_g).

Fig. 2. Circuits of the proposed high PSR LDO regulator.

Fig. 3. Analyses of power noise replication by PSRE.

Fig. 4. Simulated waveforms: (a) PSR, and (b) output variations during load transient test ($V_{DD}/V_{OUT} = 0.8\text{ V}/0.5\text{ V}$, $I_{OUT} = 0.1\text{ mA}$ – 100 mA).

3 Performance evaluations

The proposed LDO regulator shown in Fig. 2 was designed using a 1-V 90 nm CMOS process to support a 100 mA load current. The layout area is only 0.036 mm^2 . The input voltage range is 1.2 V – 0.8 V and the values of R_1 and R_2 can be adjusted to generate any regulated output level between 0.85 V – 0.5 V . The EA is designed to have a large operating range to meet variable output requirements. The maximum I_Q is $90\text{ }\mu\text{A}$, achieving a 99.91% current efficiency. Fig. 4(a) shows the simulated PSR performance when the input (V_{DD}) and output voltage (V_{OUT}) are set to 0.8 V and 0.5 V . Fig. 4(b) shows the output variation (ΔV_{OUT}) when the input/output voltage (V_{DD}/V_{OUT}) is set to $0.8\text{ V}/0.5\text{ V}$ and the load current (I_{OUT}) is switched between 0.1 mA and 100 mA . Owing to the high gain EA and PSRE, the proposed LDO regulator can achieve a PSR better than -57 dB at a frequency band of 0 – 1 MHz and an output variation of only 14 mV . Table I summarizes the performance comparisons between the proposed LDO regulator and several previous works, it clearly shows that the proposed LDO regulator achieves a high PSR, while achieving small output variation during load transient, and small line/load regulation simultaneously for low-voltage operation.

Table I. Performance evaluations

Parameters \ Designs	[7]	[8]	[2]	This Work
Technology (CMOS)	0.13 μm	0.35 μm	0.13 μm	90 nm
V_{DD} (V)	3	3.3	>1.15	1.2–0.8
V_{OUT} (V)	2.8	2.5	1	0.85*–0.5
Load Capacitor C_L (μF)	2.7	N.A.	4	1
Max. I_Q (μA)	98	32	50	90
Max. I_{OUT} (mA)	150	100	25	100
Current Efficiency	99.93%	99.97%	99.8%	99.91%
Line Regulation (mV/V)	1.5	N.A.	1.54	0.225
Load Regulation (mV/mA)	17.4	N.A.	0.048	0.0018
Output Variation ΔV_{OUT} @(I_{OUT1} – I_{OUT2} in mA)	15.8 mV (1–150)	N.A.	26 mV (0–25)	14 mV (0.1–100)
Response Time TR (μs)**	0.284	N.A.	2.4	0.14
PSR@1 MHz (dB)	–40	–46	–60	>-57
Area (mm^2)	0.166	0.108	0.049	0.036

* $V_{DD} > 1$ V in this case ** $TR = (C_L \times \Delta V_{OUT}) / I_{OUT(MAX@Transient\ Test)}$

4 Conclusion

A new low-voltage high PSR LDO regulator was proposed for low-voltage power managed SoCs. The proposed LDO regulator is designed using a 1-V 90 nm CMOS technology. Post-layout simulations show that the proposed LDO regulator can achieve a PSR of –57 dB at 1 MHz in case it converts an input of 0.8 V to an output of 0.5 V under a 100 mA load current. Meanwhile, the voltage spikes during 0.1 mA–100 mA load transient test was only 14 mV.

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