A 48-dB precise decibel linear programmable gain amplifier for GNSS receivers

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Abstract: A novel circuit architecture for programmable gain amplifier (PGA) is proposed, which simplifies and improves the conventional one and achieves wide precise digital decibel (dB)-linear gain control while obtaining a smaller gain error, smaller chip area and wider bandwidth with low power consumption. In the 0.18-μm CMOS process, the proposed PGA occupies less than 0.09 mm\(^2\) of chip area. From the measurements, the PGA shows a dB-linear gain range of 48 dB (−20 to 28 dB) with a gain error of less than 0.18 dB, a gain step of 0.86 dB, a maximum 1-dB compression point (IP1dB) of 10.4 dBm, and a 3-dB bandwidth of 450 MHz at the maximum gain while consuming only 5.8 mA from a 1.8-V supply.

Keywords: decibel (dB)-linear gain, variable gain amplifier (VGA), programmable gain amplifier (PGA), GNSS receiver chip

Classification: Integrated circuits

References

1 Introduction

Today, the GNSS (global navigation satellite systems) have been significantly developed. An automatic gain control (AGC) plays an important role in enlarging the dynamic range of the GNSS. A variable-gain amplifier (VGA) is a key block of AGC [1], and the performance of VGA will determine the performance of AGC.

In most applications, the VGAs are controlled by analog signals or digital words. As shown in Fig. 1(a), the conventional VGA [2] controlled by analog signals will consume more area and power to achieve dB-linear gain.Digitally controlled VGAs [i.e., programmable gain amplifiers (PGAs)] have also been discussed in some literature [3, 4, 5], but few of them achieve dB-linear control while producing smaller gain error. Many PGAs [3, 6] have adopted two-stage gain control technique which means coarse gain control (CGC) and fine gain control (FGC) to widen the gain control range. But the gain variation of the CGC or FGC will degrade the performance of the circuit. The circuit architecture introduced in [6] are shown in Fig. 1(b).

This letter presents a novel PGA with two-stage gain control technique, which employs digitally controlled attenuator for CGC and a digitally controlled dB-linear FGC circuit based on Binary-Weighted dual feedback regulation technique. This novel PGA simplifies and improves the circuit architecture mentioned in [2] and achieves precise digital dB-linear gain control with wide gain tuning range while obtaining smaller gain error, smaller chip area and wider bandwidth with low power consumption.

2 Proposed PGA topology

The block diagram of the entire GNSS receiver is depicted in Fig. 2(a). According to the GNSS requirements, the proposed PGA is required to provide linear output capacity of more than −10 dBm (0.2Vpp) determined by the full scale of the in-chip analog-to-digital converter (ADC) and gain range of more than 40 dB to offset signal dynamic range, gain variation of external components and possible gain variation of the integrated receiver due to process, temperature, and supply voltage variation. As shown in Fig. 2(b), the architecture of the proposed PGA includes a coarse gain control (CGC) block employing an R-2R resistor ladder attenuator and route selection switches, a FGC block which will be discussed later, fixed gain amplifiers (FGAs) providing 28 dB gain and an output buffer for next stage.
The conventional VGA introduced in [2] consists of an R-2R ladder attenuator and a series of variable trans-conductance stages attached to the ladder nodes, as shown in Fig. 1(a). Moreover, the conventional VGA require a complicated index generating circuit to achieve dB-linear gain which will consume more area and power. However, as shown in Fig. 2(b), only two variable trans-conductance blocks in FGC of the proposed PGA are connected to a R-2R ladder attenuator with route selection switches. It can simplify the circuit design and decrease the chip area. Meanwhile, coarse digital dB-linear gain control can be achieved by route selection switches controlled by digital words. Moreover, the FGC block discussed in chapter 3 can provide fine digital dB-linear gain control without index generating circuit.

In order to achieve the desired gain range, gain step and gain error, many VGAs [3, 6] have been realized by cascading coarse gain amplifier and fine gain amplifier. As shown in Fig. 1(b), due to the gain variation of the coarse gain amplifier or fine gain amplifier, which will change the gain setting of the VGA and will produce more gain errors, circuit implementation becomes complex and difficult for achieving accurate gain control. The proposed PGA structure can provide better performance in this aspect. Since the CGC block in proposed PGA topology consists of identical resistors and provides attenuation determined by the ratio between resistors, it provides precise attenuation against process and temperature variation. Moreover, gain variations of the FGC block and the CGC block are correlated. The gain control range of the FGC block is determined by corresponding gain step of the CGC block.

![Fig. 2.](image)

The proposed PGA topology in Fig. 2(b) buses a total of 6 bits for the control: 3 bits ($B_0B_1B_2$) for the FGC stage and 3 bits ($B_3B_4B_5$) for the switches $S_0$ to $S_{15}$ in the CGC stage. The CGC provides attenuation of 6.02 dB per step in an 48.16 dB gain control range, and FGC provides attenuation of 0.86 dB per step in a 6.02 dB gain control range.
3 Binary-Weighted dB-linear FGC

The proposed Binary-Weighted dB-linear FGC topology is based on dual feedback regulation technique as shown in Fig. 2(b). Two programmable trans-conductance amplifiers (GM₁ and GM₂) and the trans-impedance amplifier, which are employed by the FGC, form two overlapped unity gain feedback loops. The inputs of two programmable trans-conductance amplifiers are connected to any two adjacent nodes (V₁ and V₂, which equals to half of V₁) of the R-2R ladder attenuator (CGC) to set output signal voltage amplitude between V₁ and half of V₁, which means the attenuation of FGC varies from −6.02 dB to 0 dB by changing the trans-conductance of the two programmable trans-conductance amplifiers. The relationship between the attenuation of FGC and the trans-conductance of GM₁ and GM₂ is described by a small signal equivalent. Assuming the trans-conductance of GM₁ and GM₂ are Gm₁ and Gm₂, the trans-impedance of the trans-impedance amplifier is AR, V_{OUT} is given by

\[ [Gm_1(V_1 - V_{OUT}) + Gm_2(V_2 - V_{OUT})]AR = V_{OUT} \]  \( (1) \)

Assuming V₂ = V₁/2 and AR is large enough, the gain can be expressed as

\[ A_v = \frac{Gm_1 + 0.5Gm_2}{Gm_1 + Gm_2 + 1/AR} \approx \frac{Gm_1 + 0.5Gm_2}{Gm_1 + Gm_2} \]  \( (2) \)

![Fig. 3. Schematic of proposed FGC.](image)

The schematics of the proposed Binary-Weighted dB-linear FGA are shown in Fig. 3. The differential folded-cascode structure is adopted to realize the programmable trans-conductance amplifier and the trans-impedance amplifier. The common-mode feedback is adopted to stabilize the output common-mode DC voltage at a specified values. The schematic of the FGA adopting the binary-weighted switches is shown in Fig. 3. An array of transistor pairs in parallel, whose each unit consists of a transistor pair, a current tail, and a switch for activation/deactivation, is employed to achieve variable trans-conductance. The units with the multiplication factor 2^k \( (k = 0, 1, 2) \) in the GM₁ array and GM₂ array do not turn ON or OFF at the same time. Thus, by changing the control bits B₀, B₁ and B₂, the trans-conductance values of the input GM₁ and GM₂ can conversely be varied and are expressed as

\[ Gm_1 = \sqrt{2\mu_C C_{ox}(W/L)}I_1 \times (2^0B_0 + 2^1B_1 + 2^2B_2) \]  \( (3) \)

\[ Gm_2 = \sqrt{2\mu_C C_{ox}(W/L)}I_2 \times (2^0B_0 + 2^1B_1 + 2^2B_2) \]  \( (4) \)
where \((W/L)_{1,2}, I_{1,2}\) are the aspect ratios and bias currents of the input transistors as shown in Fig. 3. Assuming \(B = 2^4B_0 + 2^1B_1 + 2^2B_2\) is the digital control word, \(g_{m1} = [2\mu_nC_{ox}(W/L)_1]^{1/2}\), \(g_{m2} = [2\mu_nC_{ox}(W/L)_2]^{1/2}\), the trans-conductance can be re-expressed as

\[
G_{m1} = g_{m1} \times B
\]

\[
G_{m2} = g_{m2} \times (2^3 - 1 - B)
\]

Using Eq. (2), Eq. (5) and Eq. (6), the differential voltage gains of the FGC shown in Fig. 3 can be given by

\[
Av = \frac{g_{m1}B + 0.5g_{m2}(2^3 - 1 - B)}{g_{m1}B + g_{m2}(2^3 - 1 - B)}
\]

The voltage gain in Eq. (7) varies following the squared pseudo-exponential function \(Av = (1 + t)/(1 - t) \approx e^{2t}\) to realize the dB-linear gain by defining

\[
t = \frac{-0.5g_{m2}(2^3 - 1 - B)}{[2g_{m1} - 1.5g_{m2}]B + 1.5g_{m2}(2^3 - 1)}
\]

\(t\) and \(B\) can keep linear relationship, by defining

\[
g_{m1}/g_{m2} = 3/4
\]

According to Eq. (8) and Eq. (9), Eq. (8) can be rewritten as \(t = (B - 7)/21\). The attenuation of FGC varies from \(-6.02\) to \(0\) dB by using three control bits \(B\), which varies from \(0\) (\(B_2B_1B_0 = 000\)) to \(7\) (\(B_2B_1B_0 = 111\)). The FGC use this pseudo-exponential function expressed as \((1 + t)/(1 - t) \approx e^{2t}\) for decibel-linear gain control characteristics, which is limited to less than \(6.02\) dB with linearity error of less than \(0.09\) dB. The gain variation scheme reported in [7] follows the pseudo-exponential function expressed as \(Av = [(1 + t)/(1 - t)]^{1/2} \approx e^t\). Consequently, the squared pseudo-exponential function can provide twice the dB-linear gain range compared with the conventional pseudo-exponential function. The gain control step which is equal to \(6.02/(2^8)\) dB can be reduced by increasing \(k\), which is the number of parallel transistor pairs in the array. Meanwhile, the gain of the proposed all-NMOS transistor array FGC, which determined by the ratio between trans-conductance of GM1 and GM2, becomes process and temperature independent. In Fig. 3, due to many parasitic capacitances from GM1 array and GM2 array are introduced to the folding point of the differential folded-cascode structure, it will reduce the phase margin of the circuit. To solve this problem, a compensation circuit is adopted as shown in Fig. 2(b).

4 Measurement results

The microphotograph of the GNSS receiver chip including the proposed PGA is shown in Fig. 4(a), which is fabricated in the 0.18-µm CMOS process. The PGA occupies less than \(0.09\) mm\(^2\) of chip area and dissipates an average current of \(5.8\) mA from a 1.8-V supply. In Fig. 4(b), the proposed PGA shows a dynamic gain range of 48 dB (–20 to 28 dB) and a maximum gain error of less than \(0.18\) dB. Due to mismatch in the programmable trans-conductance arrays of the FGC, the finite trans-impedance of the trans-impedance amplifier, the more gain error is produced compared to the theoretical maximum gain error value \(0.09\) dB. In Fig. 4(c), the
measured OP1dB are $-9.6$ to $-2.8$ dBm (the IP1dB are $-31$ to $-10.4$ dBm), and the measured NF are 12 to 63 dB. From the measurement, the PGA shows that 3 dB bandwidth are 450 MHz. The performance is compared with [3], [4], [5] and [8], which is shown in Table I.

5 Conclusions

In this letter, we have proposed a PGA that simplifies and improves the conventional one and achieves precise digital dB-linear gain control while obtaining a smaller gain error, smaller chip area and wider bandwidth with low power consumption. The proposed PGA can also be used in many applications, such as medical equipment, other telecommunication systems, disk drives etc.

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