A non common-node chaotic Colpitts oscillator with negative resistance enhancement

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Abstract: A non common-node microwave chaotic Colpitts oscillator with enhanced negative resistance is introduced. Its negative resistance degradation caused by the Miller capacitance $C_{BC}$ is compensated with an optimum inductor load. The fundamental frequency $f_0$ and bandwidth of this chaotic oscillation can be improved over a normal common-base or common-collector oscillators. This design also enables power consumption reduction in the oscillator.

Keywords: chaotic Colpitts oscillator, negative resistance, fundamental frequency, power consumption

Classification: Integrated circuits

References

1 Introduction

Ever since reporting the first observation of chaos in a classical common-base Colpitts oscillator [1], chaotic circuit designs for meeting bandwidth demand at microwave communication have been highly sought after [2, 3, 4, 5, 6]. In general, a typical chaotic Colpitts oscillator suffers performance limitation by the negative influence of parasitics of transistors used, imposing a maximum on fundamental frequency $f_0$ [4]. To alleviate the influence of parasitics and to improve $f_0$, various design techniques have been proposed including the use of parasitics as parts of the resonance loop [4], an addition of serial L and diode load to redistribute the effects of base-collector parasitic capacitance $C_{BC}$ [5], and a cascode amplifier to reduce the Miller effect at transistor $C_{BC}$ [6].

However, these improved chaotic Colpitts oscillators have a limited success in improving $f_0/f_T$ ratio and lowering power consumption. To gain an in-depth understanding of these performance issues and to explore the use of advancement in normal oscillator design techniques for chaotic circuits, it is essential to recognize commonality as well as difference in normal and chaotic oscillator design requirements. A typical non-chaotic oscillator exhibits a sharp decrease of negative resistance at high frequencies due to the Miller effect at $C_{BC}$ limiting its maximum oscillation frequency [7]. Such an effect also appears in these chaotic Colpitts oscillators and needs to be lessened. Unlike a normal narrowband oscillator at the resonance frequency, a serial resistor is often included in the oscillation loop to satisfy the requirement for a broadband chaotic oscillation conditions, leading to a low $Q$ value and high power losses in the loop. Such a broadband oscillation requirement in chaotic circuit also imposes a higher negative resistance needed than in a normal oscillator. Thus, a challenge in a chaotic circuit design is to identify a proper and sufficient negative resistance for overcoming resonator losses, reaching a start-up chaotic oscillation and optimizing $f_0$.

In this paper, we introduce a non common-node chaotic Colpitts oscillator design with two separated inductors connected at base and collector node respectively. Tuning of these inductors allows enhancing negative resistance in the chaotic oscillator to compensate for its degradation from transistor transconductance ($g_m$) at high frequencies and maximizing fundamental frequency $f_0$. A resistor connected to a base node instead of a collector node in the oscillation loop further reduces power consumption from other common-node designs. In comparison, the new design shows an improved $f_0/f_T$ ratio of 0.2 and power consumption reduction almost 50%.

2 Principle for circuit design

Figs. 1(a) and (b) represent a common-collector and a non common-node chaotic Colpitts oscillator, respectively. The novel chaotic circuit evolves from a traditional normal common-collector Colpitts oscillator by either including a resistor $R_S$ to the base node or a combination of $R_S$ and an additional inductor load $L_C$ at the collector node. The bias current $I_{SS}$ is controlled by tuning the voltage source $-V_{SS}$. In contrast to a standard common-base chaotic Colpitts design in [1, 2, 5, 6], the proposed circuit has two important design features. Firstly, the parallel equiv-
alent inductance of the L_S-R_S and L_C-C_BC is smaller than that of individual L_S and L_C. Without significantly impacting the fundamental frequency \( f_0 \), the \( g_m \) of the transistor can be enhanced by increasing L_C value. Consequently, the negative resistance is enhanced through increasing the voltage swing between the junctions and the \( g_m \) of the transistor. Secondly, instead of having a resistor at the collector node for satisfying the chaotic oscillation requirement, the serial resistor R_S is implemented at the base node. The removal of resistor at collector node and the enhancement of \( g_m \) with L_C reduce a demand of higher V_DD, thus lowering the resonator power consumption.

3 Negative resistance analysis

The input impedance between base and collector nodes can be viewed as an equivalent circuit of a negative resistance \( R_{in} \) in series with a capacitance \( C_{in} \). From simplified calculation, \( R_{in} \) of the two circuits are as follows:

\[
R_{in}^a = -\frac{g_m}{\omega^2 C_0 C_2} \cdot \frac{1}{\left(1 + \frac{C_{BC}}{C_0} + \frac{C_{BC}}{C_2}\right)^2 + \left[\frac{g_m C_{BC}}{\omega C_0 C_2} - \frac{1}{\left(1 - \frac{C_{BC}}{C_0} + \frac{C_{BC}}{C_2}\right)^2}\right]} \tag{1}
\]

\[
R_{in}^b = -\frac{g_m}{\omega^2 C_0 C_2} \cdot \frac{1}{\left[1 + \frac{1}{1 - k}\left(\frac{C_{BC}}{C_0} + \frac{C_{BC}}{C_2}\right)\right]^2 + \left[\frac{g_m}{\omega C_0} \cdot \frac{1}{1 - k}\left(\frac{C_{BC}}{C_0} - k\right)\right]^2} \tag{2}
\]

Where, \( C_0 = C_1 + C_{BE}, k = \omega^2 L_C C_{BC} \), when \( L_C = 0 \) nH,

\[
R_{in}^a = R_{in}^b \tag{3}
\]

Equation (3) shows that equivalent circuits of the two chaotic oscillators in Fig. 1 are the same without considering L_C.

From equations (1) and (2), we can calculate the negative resistance \( R_{in} \). The transistor BFG520 with \( f_T = 9 \) GHz, \( C_{BE} = 1.2 \) pF and \( C_{BC} = 0.5 \) pF is used in calculation. Fig. 2 shows \( R_{in}^b \) and the highest chaotic fundamental frequency \( f_0 \) dependence on the ratio of \( L_C/L_S \). These two curves are generated from either fixing the \( f_0 \) and \( L_S \) values in \( R_{in} \) calculation, or fixing the chaotic start-up
condition at a preset value of $R_{in} = -35 \, \Omega$ in the $f_0$ calculation. To perform the calculation, we optimize fundamental frequency $f_0$ of the common-collector chaotic oscillator (without $L_C$) and its corresponding $R_{in}$, which are then used as reference for the subsequent calculation in the proposed non common-node oscillator to determine their dependence on the ratio of $L_C/L_S$.

The equivalent circuit of $L_C$-CBC observes capacitive and its impedance is inversely proportional to $L_C$. When $L_C$ is small, $-R_{in}$ increases with $L_C$, because the impedance of $L_C$-CBC is much larger than $-R_{in}$ and its decrease in value can be neglected. Thus, $-R_{in}$ is mainly dominated by the transistor $g_m$, which is directly proportional to the $L_C$ and the voltage and current swing in the circuit. However, when $L_C$ is large, $-R_{in}$ decreases as $L_C$ increases, because the impedance of $L_C$-CBC is too low to be neglected and because the voltage and current swing and $g_m$ enhancements become saturated. $-R_{in}$ is mainly determined by the impedance of $L_C$-CBC, decreasing with increasing $L_C$.

An optimum $L_C/L_S$ ratio is observed for the maximum negative resistance. Similarly, for a fixed $-R_{in}$, one would expected to see a corresponding $f_0$ dependence on $L_C/L_S$ ratio. This is done by adjusting $L_S$ and $C_1, C_2$ for a given $L_C/L_S$ ratio to extract the $f_0$. In Fig. 2, the highest $f_0$ and $-R_{in}$ for the common-collector version (without $L_C$) are only 1.5 GHz and 36 $\Omega$. When $L_C$ equals to 2–3 times of $L_S$, $-R_{in}$ improves by almost 52% to 55 $\Omega$. Thereby, with an optimum $L_C/L_S$ ratio, we can reduce $L_S$ and $C_1, C_2$ values to improve $f_0$ by about 47% to 2.2 GHz, as shown in Fig. 2.

4 Measurement results

The proposed non common-node (with $L_C$) and the common-collector (without $L_C$) chaotic Colpitts circuits were designed and implemented with BFG520. To optimize the fundamental frequency $f_0$, the values of the tank inductance $L_S$, $L_C$, capacitance $C_1, C_2$ and the loss resistance $R_S$ were chosen based on the concept outlined in previous sections and are summarized in the caption of Fig. 3. Note the
The effect of parasitic base-emitter capacitance $C_{BE}$ is considered in choosing $C_1$. $V_{DD}$ was fixed at 5 V and $-V_{SS}$ was adjusted to achieve the desired output chaotic signals. Fig. 3 and Fig. 4 depict the measured power spectra of the circuit without and with LC, respectively. In the experiment, the optimum LC of 2.1 times of LS is consistent with calculated results in Fig. 2. The fundamental frequency $f_0$ is 1.28 GHz and 1.779 GHz for circuits without LC and with optimum LC, respectively, illustrating $f_0$ improvement by 39%. Following the same chaotic bandwidth (BW) definition as in reference [2], the BW are 2.1 GHz (500 MHz–2.6 GHz) for the normal one and 4.6 GHz (800 MHz–5.4 GHz) for the proposed one, showing an improvement by 119%. The wire inductance and lossy parasitic resistance on the circuit board may attribute to a lower measured $f_0$ than the calculated one. Fig. 5 shows the double scroll attractor of the proposed circuit measured with oscilloscope and proves that the circuit is in completely chaotic oscillation.

Table I compares the experimental performance between the proposed design and recently published microwave chaotic Colpitts oscillators. The fundamental frequency $f_0$ and $f_0/f_T$ for the proposed design are much higher than those of the designs in [2, 5, 6]. Note that they all were implemented with BFG520. Excluding power consumption (PC) of the current source, the resonator power consumption...
(RPC) in a single-ended circuit is estimated by the product of \((V_{DD} + 0.8\, V)\) and \(I_{SS}\). RPC in this design is much lower than those single-ended circuits in [2, 5]. This power reduction is partially attributed to the removal of a resistor at collector node avoiding high collector current path and an increased \(g_m\) with an optimum collector inductor alleviating its sharp decrease at reduced bias voltage \(V_{DD}\).

### 5 Conclusion

A non common-node Colpitts oscillator with enhanced negative resistance is designed for the chaotic oscillator. Theoretical calculation shows that the negative resistance degradation at high frequencies is compensated by increasing the voltage and current swing in the circuit and the transconductance of the transistor via an optimum inductor load. With enhanced negative resistance, the experimental fundamental frequency \(f_0\) and bandwidth of the proposed circuit are 1.779 GHz and 4.6 GHz (800 MHz–5.4 GHz), respectively.

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