A novel auxiliary-free zero inductor current detection scheme for step down non-isolated LED driver

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Abstract: A novel auxiliary-free zero crossing detection (ZCD) circuit is presented in this paper, which is especially suitable for step down non-isolated LED drivers operating in boundary conduction mode (BCM). Without extra auxiliary winding, the proposed method can fast and correctly detect zero inductor current information, which only requires an integrated NMOS power switch. The step down non-isolated LED driver with the proposed ZCD scheme has been implemented in CZ6H 0.35 μm standard CMOS process, results show that the proposed ZCD scheme can always work properly regardless of the variation of line voltage and load condition.

Keywords: ZCD, LED driver, PFC, BCM

Classification: Integrated circuits

References

1 Introduction

As the high-brightness (HB) light emitting diode (LED) technology rapidly develops, their basic characteristics including high power efficiency, longevity and low maintenance requirements are more and more attractive in general lighting applications. In recent years, one of the popular solutions [1, 2, 3] to precisely regulate LED current is the single-stage active power factor control (APFC) step-down control topology, which is widely adopted in low-to-moderate power non-isolation applications.

Fig. 1(a) illustrates the simplified circuit diagram of the proposed non-isolated LED driver, which is controlled by peak current PWM method. The LEDs current estimator is compared with DC level of reference current signal \( I_{REF} \) by a low bandwidth error amplifier and then outputs a constant voltage level, which actually reacts output load condition. A sinusoidal waveform proportional to line voltage \( V_{REC} \) is utilized to control the line input current to be in phase with line voltage. Consequently, the PF value becomes very close to unity.

2 Auxiliary-free ZCD mechanism

Generally speaking, the ZCD control technique in the conventional non-isolated architectures utilized the auxiliary winding [4] to detect the instant of zero inductor current as shown in Fig. 1(b). However, it is essential that auxiliary winding occupies a large area on the PCB board. Consequently, a novel auxiliary-free ZCD mechanism is introduced in this paper. In BCM operation [2, 5], as soon as inductor current discharge to zero, a parasitic ring between the magnetizing inductor \( L_0 \) and parasitic capacitor of LDMOS occurs and the voltage signal of \( V_{Drain} \) drops dramatically.

Since the voltage level of \( V_{Drain} \) of LDMOS is as high as hundreds of volts in the discharging period, it is infeasible to directly detect the resonance waveform. As a result, a simple resonance transmitter illustrated in Fig. 2(a) is proposed here. In
the charging period, the integrated power transistor $M_0$ turns on and both LDMOS and $M_0$ operate in the deep-triode region, which can be regarded as voltage-controlled resistors. In the discharging period, power transistor $M_0$ turns off, $V_{\text{Drain}}$ is clamped by diode $D_0$ to be $(V_{\text{REC}} + V_{D0})$. Since the gate potential of LDMOS sustains a constant value ($V_{\text{DD}}$), $V_{\text{Source}}$ is thus clamped by LDMOS to be a little lower than $V_{\text{DD}}$. As soon as inductor current reaches zero, resonance phenomenon occurs at $V_{\text{Drain}}$, meanwhile, the impedance of the gate signal of LDMOS clamped by $C_{ST}$ is so low that it’s impossible for resonance signal to flow into it, as a result, resonance signal of $V_{\text{Drain}}$ would flow through the only access of parasitic capacitor $C_{DS}$ of LDMOS into $V_{\text{Source}}$. The transfer function from $V_{\text{Drain}}$ to $V_{\text{Source}}$ can be expressed as

$$H(s) = \frac{V_{\text{Source}}(s)}{V_{\text{Drain}}(s)} \approx \frac{\frac{1}{sC_{DS,M0}} + R_S}{\frac{1}{sC_{DS,L0}} + \left[ \frac{1}{sC_{DS,M0}} + R_S \right]}$$

Since the value of the sensing resistor $R_S$ is low enough to be ignored, thus formula (1) can be simplified as

$$H(s) = \frac{V_{\text{Source}}(s)}{V_{\text{Drain}}(s)} \approx \frac{C_{DS,L0}}{C_{DS,L0} + C_{GS,M0} + C_{DS,M0}}$$

Supposed that parasitic capacitor $C_{DS,L0}$ is large enough compared with parasitic capacitor $C_{DS,M0}$ and $C_{GS,M0}$, then, we can judge that resonance signal can easily be transmitted into $V_{\text{Source}}$ with little distortion. Since the drain-source breakdown voltage of LDMOS is up to 600 V, it’s credible and feasible for capacitor $C_{DS,L0}$ to transfer the resonance signal of $V_{\text{Drain}}$ to $V_{\text{Source}}$. Consequently, it’s possible to detect the zero inductor current instant by capturing the dramatic voltage drop of $V_{\text{Source}}$, because the peak voltage of it is restricted to be $V_{\text{DD}}$. 

Fig. 2. (a) Generation of resonance signal. (b) Steady-state operation waveforms of DCM operation.
3 Circuit implementation

$V_{\text{Source}}$ is the resonance signal to be sampled and detected as shown in Fig. 2(a). Fig. 3 illustrates that $V_{\text{Hold1}}$ represents the hold potential, which is sampled at the end of demagnetization period. $V_{\text{Source}}$ is compared with hold potential $V_{\text{Hold2}}$ to judge when inductor zero reaches zero, which is expressed as

$$V_{\text{Hold2}} = \frac{R_1}{R_0} (V_{\text{Hold1}} - V_{TH0})$$  \hspace{1cm} (3)

In formula (8), the scale coefficient between resistors $R_1$ and $R_0$ is supposed to be 1. As a result, the proposed ZCD topology should follow the basic principle: As soon as resonance signal $V_{\text{Source}}$ drops below the threshold voltage ($V_{\text{Hold1}} - V_{TH0}$), the comparator output changes from high level to low level and the output signal ZCD of SR latch is triggered to be high level. To avoid some unwanted pulse noise, a negative edge triggered SR flip-flop is utilized to blank the unwanted output pulse.

4 Simulation results

The chip is designed and simulated with 0.35 um standard CMOS process and the input voltage ranges from 90 V to 285 V. Fig. 4(a) shows the waveforms of inductor current, $V_{\text{Drain}}$ and $V_{\text{Source}}$ when 10 LEDs are connected in series at the output with 176 V$_{\text{AC}}$/50 Hz supply. During the inductor current demagnetization period, $V_{\text{Source}}$ acting as dc voltage is clamped by power supply $V_{DD}$ at 16.8 V. As soon as inductor current reaches zero, the potential of $V_{\text{Source}}$ drops dramatically. The delay time (around 200 ns) of ZCD trigger pulse is inevitable, which is mainly caused by judgment comparator and gate driver. From the waveforms of Fig. 4(b), we can find that the dramatic voltage drop of $V_{\text{Drain}}$ is synchronously transmitted into $V_{\text{Source}}$ with little distortion, which surely ensures the accuracy and reliability of the proposed ZCD scheme.

Fig. 5 shows the steady waveforms of line voltage $V_{\text{REC}}$ and inductor current with 176 V$_{\text{AC}}$/50 Hz supply. The top trace of Fig. 5 is the line voltage $V_{\text{REC}}$, rectifying from 35 V to 176 V. From the bottom trace of Fig. 5, we can find that the peak envelope of inductor current follows well with line voltage $V_{\text{REC}}$. Besides,
inductor current can perfectly keep BCM operation mode from valley to peak. The zero current instant is detected by the proposed ZCD technique, which determines the beginning of the next PWM signal. The operating frequency of the PWM signal varies with line voltage $V_{\text{REC}}$ from 25 KHz to 80 KHz.

![Steady operation waveforms of line voltage $V_{\text{REC}}$ and inductor current @ $V_{\text{REC}} = 176$ V, $L_0 = 1.2$ mH, $V_{\text{LED}} = 32$ V.](image)

Fig. 5. Steady operation waveforms of line voltage $V_{\text{REC}}$ and inductor current @ $V_{\text{REC}} = 176$ V, $L_0 = 1.2$ mH, $V_{\text{LED}} = 32$ V.

Fig. 6(a) shows the load and line regulation characteristic, as line rectified voltage $V_{\text{REC}}$ changes from 90 V to 285 V, the line regulation accuracy is estimated to be 3%. As the numbers of LED strings varies from 5 L to 15 L, the load regulation accuracy is estimated to be 3.3%. The power factor versus the numbers of LED strings is shown Fig. 6(b), from the results of Fig. 6(b), we can find that power factor obviously improves as the number of LED lamp increases.

The main performance summary of the proposed step-down non-isolated LED driver is shown Table I.
Conclusion

This paper proposes a novel ZCD control scheme to get rid of auxiliary winding in the step-down non-isolated LED driver. The theoretical analysis and detailed circuit implementation are illustrated in this paper. The simulation results show that the load regulation and line regulation accuracy is 3.2% and 3%, respectively. As a result, the proposed step-down non-isolated LED driver is very suitable for many lighting applications in the universal line supply systems.

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Table 1. Performance summary of the proposed LED driver

<table>
<thead>
<tr>
<th>Technology</th>
<th>CZ6H 0.35 um standard CMOS process</th>
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<tbody>
<tr>
<td>AC Input voltage</td>
<td>90~285Vac (RMS)</td>
</tr>
<tr>
<td>Numbers of LED strings</td>
<td>5 L~20 L</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>24 KHz~100 KHz</td>
</tr>
<tr>
<td>Power conversion efficiency</td>
<td>89.6% (Max) @ Vac = 220 V, 12 L</td>
</tr>
<tr>
<td>Power factor</td>
<td>&gt;0.88</td>
</tr>
<tr>
<td>Line regulation</td>
<td>3%</td>
</tr>
<tr>
<td>Load regulation</td>
<td>3.2%</td>
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Fig. 6. Simulation results of the proposed topology (a) normalized load and line regulation (b) power factor