A 1-V recycling current OTA with improved gain-bandwidth and input/output range

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Abstract: A novel bulk-driven technique is adopted to improve the gain-bandwidth of the conventional recycling current OTA, without requiring any additional power dissipation. Also, the threshold voltage of the transistors is reduced because of bulk-biasing technique, leading to the input/output voltage range extended. To compare the performance advantages of the proposed OTA versus the conventional one, two OTAs were designed in a 1-V 0.18 μm CMOS process. Results show that the proposed OTA's unit-gain bandwidth is improved by 55% and the input/output voltage range is increased by 140/110 mV. Also, the dc gain is enhanced almost 6 dB.

Keywords: bulk-biasing technique, bulk-driven technique, gain-bandwidth improvement, recycling current OTA

Classification: Integrated circuits

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1 Introduction

Operational transconductance amplifiers (OTAs) are important building

blocks for analog circuits and systems [1]. In recent years, the recycling current folded cascode (RFC) amplifier is widely used because of its improved gain-bandwidth (GBW) and dc gain [2]. However, the increasing demands in portable and biomedical applications require amplifiers of lower power consumption and lower supply voltage [3].

In an OTA, the ratio of transconductance to current consumption reflects the power efficiency. In order to obtain lower power, the efficiency of the OTA must be improved [4, 5]. In addition, with the scaling of the supply voltages, the reduction of the threshold voltage is not aggressive, which limits signal swings [6]. As a result, to extend signal swings of an OTA is necessary.

In this paper, a proposed bulk-driven recycling current folded cascode OTA (BDRFC) is presented. The bulk-driven technique is adopted to improve its gain-bandwidth without requiring any additional power. Also, the bulk-biasing technique is used to reduce the threshold voltage of the transistors, to extend the input/output voltage range. This brief is organized as follows. In Section 2, the architecture of the proposed OTA is introduced and the detailed circuit analysis is discussed. The circuit performance is next presented in Section 3, with conclusions given in Section 4.

2 The proposed BDRFC OTA

2.1 Basic topology

The conventional recycling current folded cascode OTA (RFC) is shown in Fig. 1. The input differential pairs are split in half ($M1a, b$ and $M2a, b$) and the cross-over current mirrors ($M3 : M4$ and $M5 : M6$) ensure that the

Fig. 1. Conventional recycling current folded cascode OTA (RFC)

Fig. 2. Architecture of the proposed BDRFC OTA

effective transconductance (G_m) of the RFC is improved by a ratio factor K , which leads to boost in the unity-gain bandwidth (GBW) and dc gain.

In order to further improve the GBW of the RFC, the bulk-driven technique is proposed to improve its transconductance. Also, the bulk-biasing technique is used to extend the input/output common-mode voltage range of the conventional RFC. The architecture of the proposed BDRFC OTA is shown in Fig. 2.

2.2 Unity-gain bandwidth enhancement

In bulk-driven technique, if the gate terminal is biased properly to turn on the MOS, the signal can be applied between the bulk and the source junctions so that the drain-to-source current can be modulated. Thereby a bulk terminal can behave as a second gate.

In the conventional RFC, the bulk terminal can be used to conduct the small signal current, thereby we apply the gate of the cross-over current mirror (at nodes A and B) to drive the bulk terminals of input pairs M_{ia}, b ($i = 1-2$), as shown in the red dashed lines of Fig. 2. At the same time, the bulk of the current mirror load ($M_{13} : M_{14}$) can also be used to drive the input small signal current, as shown in the red dashed lines of Fig. 2. The bulk transconductance (g_{mb}) of both the input pairs and the current mirror load contribute to the overall transconductance (G_m) and thereby increases the unity-gain bandwidth (GBW).

The bulk transconductance (g_{mb}) is expressed as,

$$g_{mb} = \eta g_m = \frac{di_D}{dv_{BS}} = \frac{\gamma g_m}{2\sqrt{2\phi_F - V_{BS}}} \quad (1)$$

reportedly, if the bulk-to-source junction is not forward biased, the ratio η ranges from 0.2 to 0.4, depending on the bulk-to-source voltage (V_{BS}) and other specific process parameters.

In the conventional RFC, the effective transconductance (G_m) is expressed as,

$$G_{mRFC} \simeq (K + 1) \cdot g_{m1b} \quad (2)$$

From Fig. 2, it can be seen that the effective transconductance (G_m) of the proposed BDRFC is expressed as,

$$G_{mBDRFC} \simeq \left[\left(\frac{g_{mb1b}}{g_{m5}} + 1 \right) \cdot (K + 1) + \frac{g_{mb14}}{g_{m5}} \right] \cdot g_{m1b} \quad (3)$$

where g_{mi} and g_{mbi} is the transconductance and bulk transconductance of transistor M_i .

When the factor K is equal to 3, the bias current (I_B) in M_{1b} is the same as that in M_5 , and I_B in M_{14} is twice that in M_5 . Considering the ratio size (W/L) of the transistors, the above Eq. (3) can be written as,

$$G_{mBDRFC} \simeq \left[\left(\eta \cdot \sqrt{\frac{K_P \cdot (W/L)_{1b}}{K_N \cdot (W/L)_5}} + 1 \right) \cdot (K + 1) + \eta \cdot \sqrt{\frac{2K_P \cdot (W/L)_{14}}{K_N \cdot (W/L)_5}} \right] \cdot g_{m1b} \quad (4)$$

From Eq. (4), it can be seen that the enhancement factor (α) is described as follow,

$$\alpha \simeq \left(\eta \cdot \sqrt{\frac{K_P \cdot (W/L)_{1b}}{K_N \cdot (W/L)_5}} + 1 \right) + \frac{1}{K + 1} \cdot \eta \cdot \sqrt{\frac{2K_P \cdot (W/L)_{14}}{K_N \cdot (W/L)_5}} \quad (5)$$

Assuming that $\eta \approx 0.3$, $K_N \approx 2 \cdot K_P$, $(W/L)_{1b} = 4 \cdot (W/L)_5$ and $(W/L)_{14} = 8 \cdot (W/L)_5$, thereby the enhancement factor α is equal to 1.6. Thus, compared to the conventional RFC, the proposed BDRFC using the proposed bulk-driven technique theoretically increases the effective transconductance almost 60%. Also, the dc gain is enhanced almost 6 dB because of the enhanced transconductance.

2.3 Common-mode range extended

The threshold voltage of a MOS transistor as a function of the bulk-source voltage V_{BS} is given by,

$$V_{th} = V_{th0} + \gamma (\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}) \quad (6)$$

where V_{th0} is zero bias threshold voltage, γ is bulk effect factor and ϕ_F is Fermi potential. The bulk bias V_{BS} is normally $> 0V$, which numerically increases the threshold voltage. However, in the bulk-biasing technique, by biasing $V_{BS} < 0V$, the threshold voltage can be actually decreased. In the Fig. 2, the transconductance (g_m) of transistor M_{1a} is given by,

$$g_{m1a} = \frac{2 \cdot I_{B1a}}{V_{GS1a} - V_{TH1a}} \quad (7)$$

Fig. 3. The effective transconductance G_{m1a} versus the input common-mode voltage range

as analyzed above, by applying a bias voltage V_A to the bulk of $M1a$, the threshold voltage V_{TH1a} is decreased because its bulk-source voltage becomes greater than zero. Decreasing V_{TH1a} decreases its gate-source voltage V_{GS1a} , which leads to the input common-mode voltage range is extended. At the same time, g_{mb1a} is equal to ηg_{m1a} , where η depends on V_{BS} and other specific process parameters. In Fig. 3 the simulated effective G_{m1a} ($g_{m1a} + g_{mb1a}$) as a function of the input common-mode voltage range is shown for the RFC and the BDRFC. It can be seen that the input common-mode voltage range of the BDRFC is extended when compared to the RFC.

In the proposed BDRFC, the bulk of both the input pairs and current mirror load are connected to the nodes A and B, respectively. The dc level of the nodes A and B is $V_{thn} + V_{ov}$ beyond the VSS , where V_{ov} is overdrive voltage, and it is approximately 500 mV in 0.18 μm process. Thus, in 1-V supply voltage, the V_{BS} of the input pairs $M_{ia,b}$ ($i = 1, 2$) and current mirror $M13 : M14$ will not forward bias the bulk-source diode.

2.4 The stability performance

The frequency performance of the BDRFC has been influenced and the phase-margin of the BDRFC is degraded. The dominant pole of the proposed BDRFC is determined by the load capacitance as the conventional RFC counterpart. However, the first non-dominant pole of the BDRFC is lowered owing to the parasitic capacitance of the bulk terminal.

In the RFC, the first non-dominant pole is expressed as,

$$p_A \simeq \frac{g_{m5}}{C_{gs5}} \quad (8)$$

where C_{gs} is the gate-to-source capacitance. But the first non-dominant pole of the BDRFC is changed as,

$$p_A^* \simeq \frac{g_{m5}}{C_{gs5} + C_{bs2a,b} + C_{bsub2a,b} + C_{bs14} + C_{bsub14}} \quad (9)$$

where C_{bs} is the bulk-to-source capacitance, and C_{bsub} is the well-to-substrate capacitance. From Eq. (9), it can be seen that the node A/B capacitance of the BDRFC is increased owing to the bulk terminal. Thus, the first non-dominant pole is lowered, leading to the degradation of the phase-margin.

3 Simulation results and discussion

To demonstrate the performance enhancement, the two amplifiers, RFC and BDRFC, was simulated using CSMC standard $0.18\ \mu\text{m}$ CMOS process. Both of the OTAs consume a total current of $200\ \mu\text{A}$, using a supply voltage of 1-V, and deriving a capacitive load of $20.0\ \text{pF}$. The detailed aspect ratio of main transistors of the BDRFC are given in Table I.

Fig. 4 shows the simulated open-loop AC response of the RFC and BDRFC. Note that the dc gain is $72.8\ \text{dB}$ for RFC and $78.7\ \text{dB}$ for BDRFC. The dc gain of the BRFC improved almost $6\ \text{dB}$ over the RFC, which is due to the improved transconductance. Also, the GBW of the RFC and BRFC

Table I. Transistors aspect ratios of the BDRFC

Transistors	W/L ($\mu\text{m}/\mu\text{m}$)	Transistors	W/L ($\mu\text{m}/\mu\text{m}$)
$M1a, b$	32/0.5	$M2a, b$	32/0.5
$M3, M5$	6/0.5	$M4, M6$	18/0.5
$M7, M8$	6/0.18	$M9, M10$	32/0.5
$M11, M12$	64/0.5	$M13, M14$	12/0.18

Fig. 4. Open-loop AC response of the RFC and BDRFC

Fig. 5. The transient responses of the RFC and BDRFC

Fig. 6. The dc gain versus the common-mode input voltage

is 22.5 MHz and 34.1 MHz respectively. The GBW improved 55% over that of the RFC, which indeed demonstrates the proposed bulk-driven technique. As for the phase margin, the BDRFC is degraded owing to the increased parasitic capacitive at node of the first non-dominant pole.

The simulation of transient responses to 2 MHz 50 mVpp step input are shown in Fig. 5. The settling time improvement of the BRFC is due to the higher GBW and the dc gain enhancement of BRFC leads to the reduced static error.

Fig. 6 shows that the dc gain as a function of the common-mode input voltage in the RFC and the BDRFC. At 1-V power supply, a 0.66 V common-mode input range in which the proposed BDRFC has at least a 73 dB gain. When compared to the RFC counterpart, it is extended by 140 mV.

Considering process variation, ac response of the proposed BDRFC has been done under different corners, which is shown in Fig. 7. It shows that the variation of gain-bandwidth is less than 1.8 MHz and that of dc gain is less than 6.8 dB.

A comparison between the proposed BDRFC and the traditional RFC is shown in Table II where both amplifiers have the same power dissipation and the same load capacitance. From the Table II, it can be seen that the

Fig. 7. DC gain and GBW of the BDRFC under different corners

Table II. Performance summary of RFC and BDRFC

Parameter	RFC	BDRFC
Technology	0.18 μm	0.18 μm
Supply Voltage [V]	1	1
Capacitive Load [pF]	20	20
Power (Bias current) [μA]	200	200
DC Gain [dB]	72.8	78.7
GBW [MHz]	22.5	34.1
Open Loop PM [deg]	84	62
ICMR (mV)	520	660
Slew rate (average) [V/ μs]	1.8	4.2
1% settling time (average) [ns]	205	65.5
Output swing (mV)	620	730
Input Noise [$n\text{V}/\text{Hz}^{1/2}$] @1 MHz	14.2	12.5
FoM (MHzpF/ μA)	225	341

FoM of the BDRFC is 341 while that of RFC is 225, which has a significant enhancement. In addition, since the decreased threshold voltage of transistor M_{13} and M_{14} , the output swing of the BDRFC increases a 110 mV when compared to the RFC.

4 Conclusion

A proposed bulk-driven recycling current folded cascode OTA (BDRFC) is presented. Under the CSMC 0.18 μm CMOS process, two OTAs were designed. To compare the performance versus the conventional counterpart, the proposed OTA's unit-gain bandwidth is improved by 55% and the input/output voltage range is increased by 140/110 mV. Also, the dc gain is enhanced almost 6 dB.

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