Wearable advanced single chip ECG telemonitoring system using SoPC

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\textbf{Abstract:} A lot of care must be taken to choose the processor for the biomedical application to meet out the real time constrains. Also the complexity of the programming increases with the multi processing environments. The real time Operating systems can support the problem up to a particular limit based on the processor architecture. When the hard real time parameters needs higher Multi processing environment, the processor struck to a limit. This paper deals with the wearable telemonitoring and Lab on chip feature for the 12 lead ECG interpretation and analysis with maintaining the patient history in case of arrhythmia like diseases. Instead of implementing the application on a single processor or FPGA solution, it is implemented using NIOS II (Altera IP core) based multi core architecture. The System on chip consists of GPS tracking, GSM base band work and the ECG processing elements and this proposes a most user friendly and wearable single medical chip. The idea of this paper is to improve the efficiency and speed of processing of the ECG interpretation and telemonitoring by separating tasks between the processors.

\textbf{Keywords:} ECG interpretation, FPGA acceleration, wearable telemetry, MPSoC

\textbf{Classification:} Integrated circuits

\textbf{References}

1 Introduction

With reference to the American Heart Association, in the United States alone, 80,000,000 people are estimated to have one or more forms of CVD and nearly 2400 Americans die of CVD each day. Cardiac arrhythmia, defined as abnormal heart rhythms, is a very common type of CVD and is thought to be responsible for most of the sudden cardiac deaths that occur every year [2].

The most common test for a cardiac arrhythmia is an ECG. The ECG measures the electrical impulses of the heart via electrodes on the skin’s surface. However, it is difficult to diagnose many arrhythmias with a standard resting ECG, because it can only provide a snapshot of the patient’s cardiovascular activity in that particular time of testing [2]. An intermittent arrhythmia can be ignored, and physicians must rely on self-monitoring and symptoms reported by patients to support their final diagnosis. In some cases, ECG recording may go to extended period of time, may be taken in an attempt to acquire data during an occurrence of an intermittent arrhythmia [2]. This kind of process requires higher computing power for wave functions (differentiation, integration, wave smoothing etc...) and multi processing environment.

Nowadays, the high end processor and FPGA related solutions are increasing very much in the field of bio medical in case of image processing noise removal in the medical images, Signal processing, PET imaging and lot [3]. Also lot of researches is going on for choosing the high performance processors and RTOS related solutions. These kinds of solutions are enough to the places where the higher speed of process is required. But these systems lack in the multi processing capability, and cannot meet out the real time biomedical constrains [1]. Here, this project deals with both the Lab on chip and the ECG telemetry. It includes Filtering of Raw ECG data, data conversions, QRS detection, and Patient history maintenance in case of arrhythmia. If the ECG shows any disorders the GPS and GSM blocks come into action. It sends the alarm to the care givers with patient location using GPS location. Each block runs independently and coordinated with the Avalon bus arbitration. ECG samples from the MIT/BIH [7] are used to generate the test inputs. The multi processing environment is achieved using the SOPC builder from the Altera. The above tasks are separated between the processors, and coordinated for the better hardware software utilization.

2 ECG

An electrocardiograph (ECG or EKG, abbreviated from the German Elektrokardiograph) is a graphic produced by an electrocardiogram, which gives the electrical response of the heart over time.

The original ECG waveform should be interpreted very carefully. The ecg analysis system comprises of scanning the heart from the various positions both horizontally and vertically. The variations in the time interval show the abnormal behavior of the heart muscles, valves and the problem in the heart functionality [5].

Each portion of ECG signal is formulated by the various sections of the heart. The Fig. 2 shows the placement of sensor leads to the human body.
The exact placement of the leads is highly important factor to do the exact ECG interpretation. The misplacement leads the process into meaningless and dangerous [4, 5]. In this paper the ECG waveforms are generated by the ECG simulators. The Fig. 3 shows the overall block of the ECG analyzer stage.

![ECG wave form and intervals](image1)

**Fig. 1.** ECG wave form and intervals

![12 Lead sensor placement](image2)

**Fig. 2.** 12 Lead sensor placement

![ECG analysis block diagram](image3)

**Fig. 3.** ECG analysis block diagram
2.1 ECG-QRS detection
From the past, numbers of systems are already implemented for the signal processing task of the off line 12 lead ECG analyses and interpretation. All the ECG interpretation methods require highly accurate QRS complex detection from the ECG signal. The real time arrhythmia detectors monitor the patients continuously for the abnormality in ECG waveforms. They store the abnormal fragments of ECG wave forms when arrhythmia occurs. For this to happen, they need to hold the accurate QRS detection mechanism [6]. Also, one has to keep in mind that, the ECG signal from the lead is not pure but mixed with power line interferences and noise signals. In this paper we use the method of QRS detection algorithm from [7].

2.2 A QRS detection algorithm
A real-time QRS detection algorithm originally developed by Pan and Tompkins [6] was further described by Hamilton and Tompkins [7]. It uses slope amplitude and width analysis of ECG signal to detect the QRS complex. Fig. 4 shows the number of Cases and filters involved in the ECG signal analysis. First a band pass filter is used to attenuate the noise signals which is compose of high pass and low pass filter. After that, the signal is passed to the differentiation, squaring, and time averaging of the signal.

Here, the filter requires only integer vales to process and avoids the complex procedure to process the floating point operations for better speed. The band pass filter attenuates the P, T waves, baseline drift, high frequency noises and power line noises. After this, the differentiation finds QRS wave in the ECG signal. These all processes are implemented with the linear digital filters. The next processes includes the squaring to make the signal positive, then it is fed to the moving window integrator it sums the area under the 150 ms square wave. The QRS complex is easily detected to find the R-R interval.

2.2.1 Band pass integer filter
The external noises due to muscle based noise, interference of 60 Hz signal, base line wander (bw), P and T wave interfaces. The 5–15 Hz range pass band maximizes the QRS energy. The recursive integer filter implemented here eliminates the zeros by locating the poles. The cascaded low pass and high pass filters used as the band pass filter.

2.2.2 Low-pass filter
The below equation is the transfer function of the second-order low-pass filter
The difference equation will be as follows

\[ y(nT) = 2y(nT - T) - y(nT - 2T) + x(nT) - 2x(nT - 6T) + x(nT - 12T) \]  

(2)

The cutoff frequency for the filter is about 11 Hz, and the delay is five samples (or 25 ms if the sampling rate is 200 sps), and the gain is about 36. The closest integer value to the gain of 36 can be implemented with simple binary shift arithmetic. This low pass filter is purely linear. It is important to note that there is more than 35-dB attenuation of the frequency when corresponding to 0.3 f/fs. We are using the sample rate of 200 sps for these filters, this represents a frequency of signal is 60 Hz. So the power line noise is attenuated also other higher frequency noises are attenuated by more than 25 dB.

### 2.2.3 High-pass filter

High pass filter can be designed by subtracting low pass filter from the all pass filter transfer function. The low-pass filter is an integer-coefficient filter with the transfer function presented as below and shown in Fig. 5.

\[ H_{lp}(z) = \frac{Y(z)}{X(z)} = \frac{1 - Z^{-32}}{1 - Z^{-1}} \]  

(3)

And the difference equation will be as follows

\[ y(nT) = y(nT - T) + x(nT) - x(nT - 32T) \]  

(4)

The dc gain of this filter is 32 and with the delay of 15.5 samples. The transfer function of the high-pass filter is given as

\[ H_{hp}(z) = P(z)/X(z) = Z^{-16} - H_{lp}(z)/32 \]  

(5)

The difference equation will be as follows

\[ P(nT) = x(nT - 16T) - (1/32)[y(nT - T) + x(nT) - x(nT - 32T)] \]  

(6)

The cut off frequency for the filter is about 5 Hz, and the delay is about 16T or 80 ms, with the gain of 1. The centre frequency is at 10 Hz. It is optimized to pass the QRS complex and lowers or attenuates the lower and higher frequency signals.
2.2.4 Derivative
After the filtering process the signal is differentiated to get the QRS complex. The transfer function of five-point derivative is

\[ H(z) = 0.1(2 + z - 1 - z - 3 - 2z - 4) \]  

This derivative can be implemented with the following equation

\[ y(nT) = \frac{1}{8}(2x(nT) + x(nT - T) - x(nT - 3T) - 2x(nT - 4T)) \]  

The 1/8 fraction is an approximation of the actual gain of the filter 0.1.

2.2.5 Moving window integral
The QRS detection cannot rely only on slope of the R wave. Many abnormal QRS complexes may come with large amplitudes and long durations which may not be detected by using the R wave only. So, we need more information from the signal to detect the QRS complex. The moving window integration gets more features in addition to the slope of the R wave. It is implemented by the following difference equation:

\[ y(nT) = \frac{1}{N}[x(nT - (N - 1)T) + x(nT - (N - 2)T) + \cdots + x(nT)] \]  

where N is the number of samples in the width of the moving window. The parameter value of this parameter should be chosen carefully to avoid the false dual QRS detection and to avoid the T wave integration with QRS complex. With the sample rate of 200 sps, 30 samples wide window was with 150 ms.

3 Proposed algorithm
The proposed algorithm provides multi-level technique for QRS detection. The three main source of distortion in QRS detection is based on noise induced in line, arrhythmia and patient [8]. The existing pilot system adapt to algorithm of closest result (i.e. it will choose any one detector if there is distortion caused by two source) which will degrade the performances. In the proposed modified pilot algorithm, the QRS detector is based on the multiple detectors in accordance with noise parameter which is given below.

3.1 Modified pilot algorithm

Case 1:
if \(<L \text{ and } bw \text{ and } ma \text{ and } SNR > -5 \text{ dB}>\)
if \(<bw \text{ and } ma>\)
then \(<\text{Choose Gritzali’s and Pan QRS Detector}>\)
else \(<\text{Choose Gritzali’s QRS Detector} >\)
else \(<\text{Default} >\)
Case 2:
if \(<L \text{ and } bw \text{ and } em \text{ and } SNR > -5 \text{ dB}>\)
if \(<bw \text{ and } em>\)
then \(<\text{Choose Gritzali’s and df2 QRS Detector}>\)
else \(<\text{Choose Gritzali’s QRS Detector} >\)
else \(<\text{Default} >\)
Case 3:
Since the impression of the proposed algorithm is same for all cases, the description is limited to case [1, 7, 8, 9]. In first case the bw and ma noise which is due to line distortion is experienced and the proposed algorithm choose Gritzali’s and Pan QRS detector whereas in existing algorithm choose only Gritzali’s detector only. In case 8 the df2 and Gritzali’s QRS detector is selected for experienced parameters. The notation stands as follows N-Normal, A-Atrial premature beat, P-Paced beat, R-Right bundle branch block beat, L-Left bundle branch block beat. In case 7, df2 and Pan detector is used for the parameter caused by arrhythmia distortion. Finally the default condition chooses the Gritzali’s detector since it is well suited for all the parameters with exceptions.

### 4 Implementation of proposed system

With the multi processing environment we could separate the overall task
among processors. The proposed system has three processing element and a hardware accelerator unit. The implementation of proposed system has three parts.

1. ECG data acquisition and algorithm selection with respect to the input ECG property done through CPU_0.
2. ECG analyzing and chronicle recognition of incoming signal for the arrhythmia detection which is done through the CPU_1.
3. The third process external communication with GPS and GSM coordinated by CPU_0.

The Fig. 6 shows the overall block diagram of the proposed system. The Altera SOPC builder provides the stage for both the user defined and inbuilt IP (Intellectual Property) core. Hence, a user can build their own hardware as IP and integrate to the system. Here we use both the methods. The built in CPU (NIOS-II) cores, memory controller, JTAG UART are used along with SRAM controller for CPU_0 store rule base for algorithm selection and for CPU_1 to store algorithms, External ADC controller and the GPS acquisition unit which are designed for this work and integrated to the system.

![Fig. 6. Overall Block Diagram](image)

The CPU_0 and CPU_1 are working in parallel for ECG data acquisition and analysis. The ECG signals are digitized using an external ADC and fed to the system through serial port. The CPU_0 and CPU_1 get the ECG signals from the external ADC. CPU_0 samples the signals and checks for the suitable QRS detector algorithm for the current incoming ECG signals. And activates the particular algorithm based on the rules specified for the better ECG classification that is piloting the suitable algorithm. The CPU_1 gets the same samples from the ADC and does the analysis process. The analysis composed of filtering, QRS detection and P-wave classification. These processes are done with Pan [6], Gritzali’s [8] and df2 [9] method which is decided on the run time based on the incoming ECG signals by the CPU_0. After the analysis, if any abnormal heart activity is detected, the CPU_0 activates GPS unit and the ECG time
fragments are send to the care giver with the GPS location through the GSM. The GSM is interfaced through the UART. The GPS unit is implemented with three major receiver components the channel, acquisition unit and tracking loops. They approximately take 1500, 3000, and 6000 logic elements respectively.

5 Results and analysis

The proposed system integrates ECG interpretation and alert system through the GSM with GPS data’s. First we analyzed the QRS detection algorithms for their efficiency in terms of False Negative FN (missed QRS complex) and False Positive FP (False alarms). Number of errors Ne (FP +FN) calculated in each algorithm for efficiency comparison. The error rate is Er = Ne / NQRS, where NQRS is the total number of actual QRSs. We studied the Ne values up to 16,000 Ne values. To test the piloting between the QRS algorithms 5 ECG’s were generated from the MIT-BIH database [7]. Each ECG took 25 to 30 min with the total of about 2.5 hours. The Table I shows the performance comparison of the each algorithm.

<table>
<thead>
<tr>
<th>ECG Score</th>
<th>Ne 1</th>
<th>Ne 2</th>
<th>Ne 3</th>
<th>Ne 4</th>
<th>Ne 5</th>
<th>Total Ne</th>
<th>Er (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pan</td>
<td>18</td>
<td>88</td>
<td>232</td>
<td>302</td>
<td>361</td>
<td>1,001</td>
<td>14</td>
</tr>
<tr>
<td>Gritzali’s</td>
<td>18</td>
<td>150</td>
<td>375</td>
<td>352</td>
<td>290</td>
<td>1,185</td>
<td>18</td>
</tr>
<tr>
<td>df2</td>
<td>310</td>
<td>250</td>
<td>168</td>
<td>158</td>
<td>310</td>
<td>1,196</td>
<td>18</td>
</tr>
<tr>
<td>Pilot</td>
<td>18</td>
<td>96</td>
<td>180</td>
<td>161</td>
<td>301</td>
<td>756</td>
<td>9</td>
</tr>
</tbody>
</table>

The experimental result reveals that, Pan, Gritzali, df2 algorithms are reliable only in ma, bw, em noise respectively. As explained in section 3. The pilot algorithm effectively adapts to the suitable detector for experienced parameter in point of fact. The Table I clearly shows the improvement in the efficiency of the Pilot system with reduced Ne and Er. The other table shows the performances computation of different types of implementation. The area and computation time for the SoPC implementation is reduced comparatively than FPGA realization. The throughput is increased remarkably in SoPC recognition with the power consumption of

<table>
<thead>
<tr>
<th>Implementation</th>
<th>Area (No. of LE)</th>
<th>Throughput (Gbps)</th>
<th>Power (mW)</th>
<th>Computation Time (Sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>2317</td>
<td>552.53</td>
<td>5.17</td>
<td>5.633</td>
</tr>
<tr>
<td>SoPC</td>
<td>1974</td>
<td>636.76</td>
<td>3.45</td>
<td>4.973</td>
</tr>
</tbody>
</table>
3.45 (mW) which is far away from power consumed by FPGA implementation.

6 Conclusions and future work

ECG interpretation using the MPSoC concept is implemented on a single chip to fulfill the requirement of wearable telemetry system for cardiac patients. And the performance in the multi processor environment was studied. The experimental results shows the MPSoC based solution increases the performance of the system by the factor of approximately 3 times. Also we compared the various QRS algorithms with our proposed piloting system in run time decision making to select the QRS algorithm. Results show the significant increase in efficiency with the reduced error rate. The system is created with reconfigurable NIOS architecture, hence it can be easily modify or components in the system. Hence it is not limited to ECG analysis. In future, we could add any number of processors, components with the application requirements.