A 0.2 V–1.8 V 8T SRAM with Bit-interleaving Capability

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Abstract: An 8T SRAM with bit-interleaving capability is designed for ultra-dynamic voltage scaling applications. An adaptive body-biasing scheme is designed to improve the stability of 8T cell, which achieves 1.5 times higher noise margin compared to the non-body-biased 8T cell. Also, a write driver is presented to enable the bit-interleaving structure, thus achieving high soft-error tolerance. A prototype 1-kb SRAM is fabricated in a standard 0.18 μm CMOS process. The measurement results show that the proposed design fulfils the functionality under supply voltage from 1.8 V to 0.3 V (0.2 V when the write wordline is boosted to 0.36 V) and the total power is reduced by four times of magnitude.

Keywords: ultra-dynamic voltage scaling (U-DVS), subthreshold SRAM, 8T cell, bit-interleaving

Classification: Integrated circuits

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1 Introduction

Ultra-dynamic voltage scaling (U-DVS) has been regarded as an effective approach to reduce energy consumption while maintaining high performance by adjusting the system supply voltage (V_{DD}) over a wide range [1]. For the ultra-low-power SoCs such as biomedical systems, sensor networks, space and military hardware, embedded SRAMs are popularly used and occupy a significant portion of total chip area and total chip power in SoCs. For the whole system, analog and RF modules also need to be integrated on the chip, which may impede the usage of high level technology. So a U-DVS enabled SRAM based on 0.18- μm standard CMOS technology is designed in this express.

Conventional 6T SRAM suffers from static noise margin (SNM) degradation in subthreshold region [2]. In work [3, 4, 5], 8T, 9T and 10T cells are presented to enhance the read stability, thus cells could well operate in subthreshold region. However, soft-error problem becomes more critical in subthreshold SRAMs [6]. Soft-error rate (SER) increases by 18% for every 10% reduction of V_{DD} [7, 8]. Bit-interleaving technique is a good way to enhance soft-error immunity by physically interleaving bits of data from different words. However, subthreshold cells designed in [3, 4, 5] suffer from the half-selected problem if bit-interleaving is used. To implement bit-interleaving, a fully differential 10T cell is proposed in [9] at the expense of area overhead and a differential 8T cell is designed in [10] by adopting a column-based dynamic cell-supply.

Another issue is that the aforementioned SRAMs [3, 4, 5, 9, 10] could not operate efficiently at higher voltages since they were all targeted for the subthreshold operation. Actually, the characteristics of MOSFETs in the subthreshold region are significantly different from those in the super-threshold region, which brings challenges for the U-DVS SRAM design. In [11], a U-DVS enabled 8T SRAM is presented. But it also suffers from half-selected disturbance if bit-interleaving technique is utilized.

This express presents a 0.2V–1.8V 8T SRAM with bit-interleaving capability. Over this supply range, the total power dissipation per access scales down by 2.2×10^4 times. An adaptive body-biasing circuit is designed to get 1.5 times higher SNM. Moreover, a write driver is designed to avoid the half-selected disturbance, thus bit-interleaved structure can be successfully implemented. By improving the peripheral circuit, this bit-interleaving scheme provides less restriction to cell topologies.

2 Enhanced 8T cell with adaptive body-bias for U-DVS SRAM

To reduce the cell area, the minimum geometry devices are used in this work. Simulations of read SNM show that the 8T cell [3] with minimum geometry loses its stability at fast NMOS and slow PMOS corner (fs corner). Enlarging size of the pull-up transistor could get a balanced P/N ratio. However, it induces 7 times larger width for the pull-up transistors when 8T cell operates in the subthreshold region [12]. Besides, large size of pull-up transistors reduces the write margin.

In this work, a forward body-bias is applied to the pull-up transistors (MP1 and MP2), as shown in Fig. 1(a), where V_{pb} represents the voltage difference between the source and the bulk of the pull-up transistor. Simulations of read SNM are performed by using standard 0.18 μm CMOS technology for the body-biased 8T cell and non-body-biased 8T cell under different corners when V_{DD} changes from 0.2 V to 1.8 V. Simulation results show that the read SNM of the body-biased 8T cell increases with V_{DD} and keeps positive at all corners. The body-biased 8T cell shows an average of 1.5X improvement of read SNM than non-body-biased 8T cell in the subthreshold region at fs corner if minimum geometry of MOSFETs is used.

However, the forward body-bias of PMOS transistor in the cell reduces write ability and increases leakage in the super-threshold operations. An adaptive body-biasing circuit is designed to solve this problem, as shown in Fig. 1(b). *Vsel* signal is ‘1’ when V_{DD} is below 0.9 V and keeps ‘0’ when V_{DD} is above 0.9 V. *Write* signal is ‘1’ for the write operation. The body-biasing circuit is shared by a row of memory cells. When a row of cells is accessed to write or V_{DD} is above 0.9 V, the body-terminals of PMOS transistors in the cell will be connected to V_{DD} to maintain the write ability and maintain low leakage. Otherwise, the body-terminals of PMOS transistors in the cell are connected to V_{bias} ($V_{bias} = V_{DD} - V_{pb}$).

Fig. 1. (a) Body-biased 8T cell and (b) adaptive body-bias circuit.

3 Bit-interleaving structure for U-VDS SRAM

With the scaling down of V_{DD} , soft-error rate (SER) caused by the particle strike increases significantly due to the reduction of critical charges in weak inversion region of MOSFETs. Bit-interleaved architecture is preferred due to the enhanced soft-error tolerance and better sense-amplifier (SA) utilization. In Fig. 2(a) and (b), non-interleaved and bit-interleaved architectures are exemplified, respectively.

In Fig. 2(a), when WL is activated during access, all the bits on the row are turned on. As an example, if A0 is attacked by the particles, A1 and A2 are probably erroneous too, which may bring multi-bit error in word A. Multi-bit error cannot be efficiently solved by conventional error correction coding (ECC). It requires much more complicated multi-bit ECC scheme, which brings extra cost in area and time-delay. However, in Fig. 2(b), if A0 is

attacked, since A0, A1, and A2 are physically separated, only single-bit error arises in word A, which can be easily addressed by the conventional ECC methods. In addition, as shown in Fig. 2(b), bit-interleaved architecture also enables the sharing of SA circuits, which increases the area-efficiency.

Fig. 2. SRAM architecture (a) non-interleaving and (b) bit-interleaving.

However, bit-interleaving structure cannot be directly utilized in the previous subthreshold SRAMs [3, 4, 5] because the row-selected but column-non-selected cells, i.e., half-selected cells, suffer from data disturbance in the write mode. Fig. 3 illustrates the half-selected disturbance of 8T SRAMs in [3]. During a write operation, when the write wordline (WWL) of the accessed row is asserted to ‘1’, the storage nodes of the half-selected cells are exposed to the precharged bitlines (BL and BLB) through active accessed transistors, which will result in the upset of “0” node in half-selected cells.

Fig. 3. Half-selected disturbance during write mode of 8T cells in [3].

A latched write driver (LWD) is presented to eliminate the half-selected disturbance in this work. Fig. 4 shows the block diagram of a 4-to-1 bit-interleaved architecture including the column-controlled LWDs. A row of cells consists of four logic words A, B, C, and D. Each logic word consists of four cells, i.e., x0, x1, x2, x3 (x = A, B, C or D), which are physically isolated. The number of the LWDs is equal to the number of cells in one logic word, and the number of latches in one LWD is equal to the number of logic words in a row. Hence, in this work, four LWDs are required and each LWD has four latches.

Fig. 4. (a) Bit-interleaving SRAM architecture with (b) LWD circuit.

We use Fig. 4 and Fig. 5 to explain how LWD eliminates half-selected disturbance. Fig. 5(a) shows the write mode of the 8T cell. During the write operation, WEN in Fig. 4(b) is activated to ‘0’ and the write wordline (WWL) in Fig. 5(a) is asserted to ‘1’. When a row is accessed, only one of the four logic words in this accessed row is selected depending on the column-decoded signal YC<i> (i = 0, 1, 2, 3). The 4-bit cells of the activated logic word operate simultaneously. Fig. 5(b) shows the transient simulation of the write operation. We assume that, in the first write cycle, YC<0> is asserted to ‘1’ and the logic word A is accessed. For A0, if we write ‘0’ to it, the input data ‘0’ of DIN is transferred to BL<0> through LWD and then is written into A0. In the second write cycle, the logic word B on the same row is accessed by asserted YC<1>, while YC<0> is disabled and hence A0 becomes half-selected. The disabled YC<0> makes the first latch in LWD shown in Fig. 4(b) enter the latched status. As a result, the voltage of BL<0> in this period still remains ‘0’, which is the value of BL<0> in the previous period when A0 is accessed to write ‘0’. Hence, for the half-selected cell A0 in this period, there is no voltage difference between its bitlines (BL<0> and BLB<0>) and the storage nodes. The write-access transistors in A0 are therefore completely turned off owing to the zero source-drain voltage. Consequently, the half-selected disturbance is eliminated. Fig. 5(b) also shows that when WWL is boosted from 0.25 V to 0.5 V there is no half-selected disturbance. It indicates that the proposed bit-interleaving scheme is compatible with the wordline boosting technique [5] which enhances the write ability for subthreshold operation. The MC simulations are done to show the SNM comparison between half-selected cells in

Fig. 5. (a) Write mode of 8T cell in this work and (b) transient simulation results of the write operation.

this work and those in the standard 8T cell at 0.2 V V_{DD} . The stability of half-selected cells in this work is improved to get the SNM of 45 mV, which is almost the same as the hold SNM. Since the half-selected problem is solved, bit-interleaving scheme can be implemented efficiently and therefore soft-error immunity is improved.

Besides, the bit-interleaving scheme enables the multiplexing of sense amplifiers to achieve high area-efficiency and low power. A hefty amount of current is saved because only one logic word is activated, which is different from the existing designs where all cells in the accessed row operate simultaneously. Compared with the previous bit-interleaving schemes in [9, 10], the advantage of this method is that it has less restriction to the cell topology because half-selected disturbance is removed by developing LWD instead of designing a new cell. Bit-interleaving scheme in this work is not only applicable for the 8T cell but also feasible for the subthreshold 9T cell [4] and 10T cell [5].

4 Measurement results

A 64-row $\times$ 16-column test chip has been implemented using standard 0.18 μ m CMOS process. Fig. 6 shows the die photo. The chip area is about 610 μ m $\times$ 224 μ m. The test chip achieves correct function from 1.8 V V_{DD} to 0.2 V V_{DD} with the operating frequency from 208 MHz to 184 kHz. When V_{DD} is below 0.3 V, the write wordline is boosted to ensure a correct write operation. The minimum V_{DD} for successful write and read operations are both 0.2 V when the write wordline is boosted to 360 mV. Fig. 7 shows the measured access waveforms when V_{DD} is 0.2 V. A periodic test pattern of write “0”,

Fig. 6. Die photo of prototype SRAM.

Fig. 7. Measured operation waveforms at 0.2 V.

read “0”, write “1” and read “1”, etc., is applied to the test chip. The output signal (DOUT in Fig. 7) is toggled per 2 clock cycles, which demonstrates the successful access operation at 0.2 V when the write wordline is boosted to 0.36 V.

Fig. 8 shows the measurement results of frequency, leakage power, total power and energy consumption. The frequency is 184 kHz at 0.2 V and the total power is about 250 nW. From 1.8 V to 0.2 V, the total power and leakage power reduce by $\sim 2.2 \times 10^4$ X and ~ 20 X, respectively. The test chip obtains the minimum energy of 1.8 pJ at 0.3 V. The performance of the test chip is summarized in Table I.

5 Conclusion

A U-DVS-enabled 8T SRAM with robustness and bit-interleaving capability is proposed. An adaptive body-biasing circuit is designed to get 1.5X higher SNM. Half-selected disturbance in the 8T SRAM is eliminated by a latched write driver, thus the bit-interleaving structure is implemented to achieve high soft-error immunity and area-efficiency. Measurement results demonstrate the test chip operates correctly from 1.8 V at 208 MHz to 0.2 V at 184 kHz. The total power consumption at 0.2 V is only 250 nW and the minimum energy of 1.8 pJ occurs at 0.3 V. This design achieves a large V_{DD} range and scaling-down power, which is suitable for the U-DVS-enabled SoCs and energy-constrained applications.

Fig. 8. Measurement results of (a) frequency, leakage power, (b) total power dissipation and (c) energy consumption.

Table I. Performance summary of the test chip

Process	0.18 μ m
SRAM configuration	64-row $\times$ 16-column
	4-1 bit-interleaving
Operating voltage of cell	0.3 V–1.8 V (0.2 V at $V_{WWL} = 0.36$ V)
Maximum frequency	208 MHz @ 1.8 V
	184 kHz @ 0.2 V
Total power	5.6 mW @ 1.8 V
	250 nW @ 0.2 V
Minimum energy	1.8 pJ @ 0.3 V

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