Analysis and design of a V-band low-noise amplifier in 90 nm CMOS for 60 GHz applications

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Abstract: A V-band low-noise amplifier with the gain boosting and noise reduction technique in 90 nm LP CMOS is implemented and tested in this paper. The operation principles of the two techniques are analyzed in detail. The fabricated LNA has a peak gain of 19.8 dB, 3-dB bandwidth of 10.5 GHz and NF of 5.86 dB at 61.5 GHz. Additionally, the reverse isolation of this LNA is better than 50 dB at all frequency. The input and output return losses are both below -10 dB in the China's 60 GHz unlicensed band (59–64 GHz). The total chip size is 0.36 mm^2 including testing pads.

Keywords: low-noise amplifier (LNA), millimeter wave (MMW), gain boosting, noise reduction

Classification: Integrated circuits

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1 Introduction

In recent years, the unlicensed band ranging from 57 to 66 GHz has become of special interest owing to its broadband bandwidth suiting for high data rate communication. The V-band spectrum centering around 60 GHz has found an increasingly wide utilization in many high speed wireless standards and applications such as 802.11ad, 802.15c, WirelessHD, WiGig, and ROF transmission. Due to the advantages of high-level integration, low cost and low power consumption, CMOS technology is tempting to develop the 60 GHz transceiver front-ends. Low-noise amplifier (LNA) is the first active circuit of receiver, whose performance is crucial to the sensitivity and dynamic range of the overall system.

For millimeter wave (MMW) LNAs implementation, an amplifier with a multistage topology is usually adopted to increase the power gain. For example, in [1], a two-stage common source (CS) amplifier with the transformer feedback LNA in 65 nm CMOS process was reported. Though a low NF of 3.8 dB was achieved, the gain of 10 dB, and dc power consumption of 35 mW were not satisfactory. In [2], a three-stage CS amplifier with the transformer and capacitive feedback LNA in 65 nm CMOS process was demonstrated. Though a high gain of 23 dB was achieved, the reverse isolation of 37 dB was too low. Multistage common source configurations [2, 3] are widely used in MMW band due to their superior noise performance, but suffer from poor reverse isolation. Multistage cascode topology has the advantage of good isolation, however, as the operation frequency increases, the noise performance of traditional cascode amplifier will be degenerated due to the existence of large parasitic capacitance on the interstage node of the cascode structure. In [4], a parallel inductor is added at the drain of the CS transistor to resonate with the parasitic capacitance of regular cascode amplifier, thus reducing the NF of the cascode amplifier. In [5], an extra inductor is added between the CS and CG transistor to resonate with the parasitic capacitance at the interstage node, thus reducing the NF as well. In [6], a T-type matching network is placed between the CS and CG stage to solve the influence of the parasitic capacitance. In [7], an additional inductor was added at the gate of the CG transistor to improve the gain with penalty in the stability of the circuit. In [8], Terry Yao, et al. have been explored the algorithmic design methodology of MMW LNA, however their analysis on the interstage match between the CS and CG amplifier was not reasonable, and it was not satisfied with a gain of 14.6 dB, reverse isolation of 32 dB and 3-dB bandwidth of 8 GHz in their work.

In this paper, we present a V-band LNA fabricated in a 90 nm CMOS technology. This LNA utilizes the noise reduction and gain boosting technique to achieve a peak gain of 19.8 dB and NF of 5.86 dB. Moreover, the analysis of the gain boosting and noise reduction technique is also presented.

2 Circuit design and analysis

2.1 Circuit topology and transistor biasing

The V-band LNA schematic is presented in Fig. 1. The LNA is composed of a CS stage followed by two cascode stages. And two extra inductors are used in each cascode stage. One inductor (L_4 and L_8) is added between the CS and CG stage to

Fig. 1. The schematic of the presented LNA

Fig. 2. Simulated $G_{\max}$ and $NF_{\min}$ versus the current density at 60 GHz

resonate with the parasitic capacitance of active devices, thus reducing the noise contribution from the CG transistor. The other inductor (L_{g1} and L_{g2}) is added at the gate of the CG transistor, which can establish resonant tank to boost the gain at the higher frequency. However, in order to make the circuit unconditionally stable, the inductance value should not be too big.

Transistor biasing is critical to the power gain of amplifier as well as the minimum noise figure. While other authors have investigated the impact of biasing on peak f_{MAX} values and noise parameters of MOSFETs [9], it is more intuitive to determinate the biasing by comparing the relationships of maximum available gain (G_{max}) and minimum NF (NF_{min}) versus current density. The simulated G_{max} and NF_{min} of the CS amplifier versus current density are shown in Fig. 2. It is observed that the variation of NF_{min} versus current density is different from the fluctuation of G_{max} . The G_{max} is maximum when the current density is about $0.35 \text{ mA}/\mu\text{m}$, while the NF_{min} is minimum when the current density is about $0.1 \text{ mA}/\mu\text{m}$. Thus, there exhibits a trade-off between gain and noise performance in practical designs, and the current density of each stage in this work are selected about $0.2 \text{ mA}/\mu\text{m}$.

2.2 Analysis of the traditional cascode amplifier

Fig. 3 shows the schematic and equivalent small-signal circuit of traditional cascode amplifier. The impedance Z_L is the output load, and the capacitor C_X is the total parasitic capacitance to ground at the node X of this amplifier. C_X will

Fig. 3. The schematic and equivalent circuit of traditional cascode amplifier

deteriorate the noise and gain performance of conventional cascode amplifier in the higher frequency, especially in the MMW band.

To simplify the analysis, the effect from the gate induced noise, gate-drain capacitor C_{gd} and channel length modulation be neglected, the noise factor of the classical cascode amplifier is given as [4]

$$F_{cas} = 1 + \gamma_1 g_{do1} R_S \left(\frac{\omega_o}{\omega_T} \right)^2 + 4\gamma_2 g_{do2} R_S \left(\frac{\omega_o C_X}{g_{m2}} \right)^2 \left(\frac{\omega_o}{\omega_T} \right)^2 \quad (1)$$

Where $g_{do1(2)}$ and g_{m2} are the drain to source conductance of $M_{1(2)}$ at zero V_{ds} and the transconductance of M_2 , respectively. $\gamma_{1(2)}$ is the bias-dependent parameter for $M_{1(2)}$. $\omega_T = g_{m1}/C_{gs1}$, and ω_o is the input resonant angular frequency. R_S is the source impedance. And the voltage gain of traditional cascode amplifier is given as

$$A_{v,cas} = - \frac{G_{m1} g_{m2} Z_L}{g_{m2} + S C_X} \quad (2)$$

Where G_{m1} is the equivalent transconductance of the CS stage, and it is shown as

$$G_{m1} = \frac{\omega_T}{\omega_o R_S} \quad (3)$$

2.3 Operation principle of the noise reduction technique

In [8], Terry Yao, et al. presented adding an inductor in cascode stage to boost the f_T of cascode, but they thought this technique as the artificial transmission line match, which is not reasonable. The artificial transmission line is usually comprised of more than T-sections or π -sections. Since the interstage match is only one π -section in this technique, the match network is not an artificial transmission line. Fig. 4 shows the schematic and equivalent small-signal model of cascode amplifier with this technique. The noise factor of cascode amplifier with a noise reduction inductor can be written as follows.

$$F_{nr} = 1 + \gamma_1 g_{do1} R_S \left(\frac{\omega_o}{\omega_T} \right)^2 + 4\gamma_2 g_{do2} R_S \left(\frac{\omega_o C'_X}{g_{m2}} \right)^2 \left(\frac{\omega_o}{\omega_T} \right)^2 \quad (4)$$

$$C'_X = (C_1 + C_2) \left[1 - \omega_o^2 L_{d1} \frac{C_1 C_2}{C_1 + C_2} \right] = C_X \left[1 - \omega_o^2 L_{d1} \frac{C_1 C_2}{C_X} \right] \quad (5)$$

Where C_1 and C_2 represent the parasitic capacitor to ground at the drain of transistor M_1 and at the source of transistor M_2 , respectively. C_X is the sum of

Fig. 4. The schematic and equivalent small-signal model of cascode amplifier with the noise reduction technique

Fig. 5. Simulated the NF_{min} and G_{max} versus the inductor L_{d1} at 60 GHz

C_1 and C_2 . L_{d1} is the noise reduction inductor. According to Eq. (4) and Eq. (5), when the inductor L_{d1} resonates with the parasitic capacitors ($L_{d1} = C_X/\omega_o^2 C_1 C_2$), the noise contribution from the transistor M_2 will be reduced effectively and then the total noise of the circuit can be decreased. After the small-signal analysis, the voltage gain of the cascode amplifier with the noise reduction technique can be written as

$$|A_{v,nr}|^2 = \frac{(-G_{m1}g_{m2}Z_L)^2}{g_{m2}^2(1 - \omega_o^2 L_{d1} C_1)^2 + \omega_o^2 C_X^2 \left(1 - \omega_o^2 L_{d1} \frac{C_1 C_2}{C_X}\right)^2} \quad (6)$$

Eq. (6) suggests that the gain of amplifier with the noise reduction technique increases slightly with respect to the inductor L_{d1} , and then declines gradually. When differentiating the denominator of Eq. (6) with respect to L_{d1} , one obtains

$$L_{d1} = \frac{g_{m2}^2 + \omega_o^2 C_2 C_X}{\omega_o^2 C_1 (g_{m2}^2 + \omega_o^2 C_2^2)} = \frac{C_X \left(\frac{g_{m2}^2}{C_X} + \omega_o^2 C_2\right)}{\omega_o^2 C_1 C_2 \left(\frac{g_{m2}^2}{C_2} + \omega_o^2 C_2\right)} < \frac{C_X}{\omega_o^2 C_1 C_2} \quad (7)$$

The amplifier will achieve the maximum gain when satisfy the Eq. (7). The simulated NF_{min} and G_{max} of cascode amplifier with this technique versus the inductance value of L_{d1} are shown in Fig. 5. It is observed that the simulated NF_{min}

and $G_{\max}$ of the amplifier agree with the above analysis greatly. The simulated $G_{\max}$ is maximum when the inductance value of L_{d1} is about 150 pH, while the simulated $NF_{\min}$ is minimum when the inductance value of L_{d1} is about 350 pH, which implies that there will be some compromises in practical designs. To obtain better noise and gain performance simultaneously, the inductance value of L_{d1} is selected about 200 pH.

2.4 Operation principle of the gain-boosting technique

Fig. 6 shows the schematic and equivalent small-signal circuit of cascode amplifier with the gain-boosting technique. By the small-signal analysis, the voltage gain of the amplifier can be given as

$$|A_{v,gb}|^2 = \frac{(-G_{m1}g_{m2}Z_L)^2}{g_{m2}^2 + \omega_o^2(C'_1 + C'_2)^2(1 - \omega_o^2L_{g2}C'_1C'_2)^2} \approx \frac{(-G_{m1}g_{m2}Z_L)^2}{g_{m2}^2 + \omega_o^2C_X^2(1 - \omega_o^2L_{g2}C'_1C'_2)^2} \quad (8)$$

Where C'_1 and C'_2 are the parasitic capacitance of the transistors. Compared Eq. (8) with Eq. (2), it is clear that the inductor L_{g2} can enhance the gain of circuit effectively, when the inductor L_{g2} is resonated with the parasitic capacitors. However, the inductor L_{g2} will deteriorate increasingly the stability as well. The simulated $G_{\max}$ and K-factor of this amplifier versus the inductor L_{g2} are shown in Fig. 7. To obtain better gain and stability simultaneously, the value of L_{g2} is selected about 50 pH.

Fig. 6. The schematic and equivalent small-signal circuit of cascode amplifier with the gain-boosting technique

Fig. 7. Simulated the $G_{\max}$ and K-factor versus the inductor L_{g2} at 60 GHz

Fig. 8. Simulated the K-factor versus the inductor L_{d1} and L_{g2} at 60 GHz

2.5 Stability analysis of the two techniques

Fig. 8 shows the K-factor of cascode amplifier with the two techniques respectively. It is obvious that the gain boosting inductor L_{g2} deteriorates the stability seriously, and the noise reduction inductor L_{d1} improves the stability slightly. The reason can be explained by deriving the input admittance of the circuit. The input admittance of the CG stage with the gain boosting technique in Fig. 4 is written as

$$Y_{IN2,gb} = \frac{g_{m2} + S(C'_1 + C'_2) \left[1 + S^2 L_{g2} \frac{C'_1 C'_2}{C'_1 + C'_2} \right]}{1 + S^2 L_{g2} C'_2} \quad (9)$$

$$\text{Re}[Y_{IN2,gb}] = \frac{g_{m2}}{1 - \omega_o^2 L_{g2} C'_2} \quad (10)$$

Eq. (10) indicates that the excessively large inductor L_{g2} will lead to a negative conductance in the input admittance, thus the circuit is unstable. Similarity, the input admittance of the CG stage with the noise reduction technique in Fig. 6 is given as

$$Y_{IN2,nr} = SC_1 + \frac{g_{m2} + S(C_1 + C_2)}{1 + Sg_{m2}L_{d1} + S^2 L_{d1} C_2} \quad (11)$$

$$\text{Re}[Y_{IN2,nr}] = \frac{g_{m2}}{(1 - \omega_o^2 L_{d1} C_2)^2 + \omega_o^2 g_{m2}^2 L_{d1}^2} \quad (12)$$

From Eq. (12), it is observed that a negative input conductance could not be obtained in any case, thus the amplifier with the noise reduction technique will be stable unconditionally.

3 Measurement results

The proposed LNA was designed and fabricated in a 90 nm LP CMOS technology. The chip occupies 0.36 mm² area including testing pads and is depicted in Fig. 9. The LNA was tested by Agilent PNA-X N5267A up to a frequency of 67 GHz. Fig. 10 and Fig. 11 illustrate the measured and simulated S parameters of the presented amplifier. For a supply voltage of 1.2 V, the measured peak S21 is lower than the simulated peak S21 about 6.5 dB, which may be caused by the inaccurate model and the parasitic effect of the long and narrow supply paths. Since the model using for this LNA design was verified and demonstrated only in below 30.1 GHz

Fig. 9. The micrograph of the proposed LNA

Fig. 10. Simulated and measured S21 and NF versus frequency

Fig. 11. Simulated and measured S11, S22 & S12 versus frequency

by the manufacturer, the model at 60 GHz is more likely inaccurate. For different supply voltages, the gain measurement results are shown in Fig. 12. The measured peak gain for the supply voltage of 1.2 V, 1.5 V, and 2 V are 13.3 dB, 16.3 dB, and 19.8 dB, respectively. The measured results can agree with simulation greatly when the supply voltage is 2 V, thus the next measurements are tested with a 2 V supply. It can be observed in Fig. 10 that the LNA has a peak gain of 19.8 dB at 61.5 GHz and 3-dB bandwidth of 10.5 GHz. For the lack of noise figure analyzer, the noise figure of this LNA was not measured. The simulated NF is lower 6.4 dB from 54 to 66 GHz and the minimum simulated NF is 5.86 dB at 60 GHz. In addition, the measured reverse isolation is lower than -50 dB. The input and output return losses

Fig. 12. Measured gain versus frequency for different supply voltages.

Fig. 13. Simulated and measured stability versus frequency

Fig. 14. Measured input 1 dB compression point at 60 GHz

are both below -10 dB from 58 to 65 GHz. Fig. 13 shows the measured results of stability. It is observed that the presented LNA is stable unconditionally. Fig. 14 shows the input 1 dB compression point of this amplifier is about -22 dBm. Table I shows the performance summary and comparison with previously reported MMW LNA.

Table I. Recently reported CMOS MMW low noise amplifiers

Ref.	Tech. (nm)	f_T (GHz)	Peak Freq. (GHz)/ BW _{3dB} (%)	Peak Gain (dB)	S12 (dB)	NF (dB)	IP _{-1dB} (dBm)	P _{DC} (mW)	Area (mm ²)	†FOM
[1]*	65	145	61/37**	10	>47	3.8	−4.6	35	0.94	10
[2]	65	N/A	58/15	23	>37	4	−26	8 (1.25 V)	0.05***	N/A
[3]	90	95	45/13	18.3	>40	4.73	−15	20 (1.2 V)	0.57	12.9
[5]	65	250	58/23	16	>40	4.5	−23	10 (2 V)	0.25***	18.4
[6]	90	95	60/N/A	7.5	N/A	6.5**	N/A	6.7	0.34	N/A
[7]	65	250	60/20	18	>40	4	−22	28.8 (1.2 V)	0.54	8.77
[8]	90	120	58/14	14.6	>32	5.5	N/A	24 (1.5 V)	0.14	5.85
This work	90	95	61.5/17	19.8	>50	5.23**	−22	26 (2 V)	0.36	17.8
	90	95	61.5/17	16.3	>50	5.41**	−20	16.5 (1.5 V)	0.36	17.7
	90	95	61/17	13.3	>50	5.86**	−20	9.6 (1.2 V)	0.36	18.3

*: measured with the source resistance of 30 Ω; **: simulated results; ***: core area without pads.

$$†: \text{FOM} = \frac{\text{Gain} \times \text{BW (GHz)}}{[\text{NF} - 1] \times P_{\text{DC}} \text{ (W)} \times f_T \text{ (GHz)}}$$

4 Conclusions

A V-band LNA for 60 GHz application has been demonstrated in this paper. By connecting an additional inductor in series between the CS and CG stage of cascode configuration, the noise contribution from CG transistor can be decreased, thus reduce the total noise of cascode amplifier. In addition, an extra inductor is utilized at the gate of the CG stage to boost the gain of cascode amplifier. Experimental results show a peak gain of 19.8 dB with 3-dB bandwidth from 56 to 66.5 GHz, and IP_{1dB} of −22 dBm, while consuming 26 mW from a 2 V supply.

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