Sudden-voltage-drop protection technique for enhancing the reliability of mobile devices under low battery conditions

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Abstract: When there is an impending heavy workload under low battery conditions, mobile device such as smartphones can autonomously reset or even shut down to prevent damage caused by sudden voltage drops. Recently, the occurrence probability of sudden voltage drop under low battery conditions has increased with the use of high-performance 64-bit CPU cores, which adversely affects the user experiences. To overcome this problem, we propose a cost-effective sudden-voltage-drop protection (SVDP) technique to minimize unstable states, thus enhancing customer satisfaction. Programmable low-battery-state-aware logic for sudden voltage drop detection and performance tuning to maintain system stability via clock frequency control is incorporated in power management integrated circuit (PMIC) and application processor (AP). Experimental results show that the proposed technique significantly reduces the failure rate due to sudden voltage drops under low battery conditions.

Keywords: application processor, low battery condition, sudden voltage drop, clock frequency control, mobile device

Classification: Electron devices, circuits, and systems

References


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1 Introduction

In battery-powered devices, graceful degradation under impending energy starvation is one of important factors for user satisfaction in terms of quality of service. Consequently, the unique discharge profile characteristics of the battery, such as rate capacity and recovery effects, are now utilized in low battery conditions. For example, power management IC (PMIC) might reset or halt the mobile device to avoid the damage caused by sudden voltage drop using the under voltage lockout (UVLO) circuit if the battery voltage level drops lower than a specified value [1]. However, sustaining the stability against sudden voltage drop is becoming more challengeable because the increased rate of power dissipation of leading-edge multi-core application processors (APs) is faster than that of Li-ion battery capacity [2]. With the advent of higher performance APs with 64-bit CPU cores, power consumption has increased by up to 20 percent for the same clock frequency when compared to the previous generation (i.e., 32-bit CPU cores) [3].

It is well known that the demand for battery life extension is ever-increasing in our daily life. Furthermore, let us think of an emergency situations in which you try to communicate with other people or take photos to indicate your location for rescue when your battery is nearly depleted. Therefore, the maximization of the remaining battery capacity under low battery conditions has compelling reason.

Because of the nonlinear discharge characteristics of batteries, especially in low energy conditions, a new cost-effective low-battery-state-aware power management scheme that does not interfere with existing low power techniques is needed. Therefore, we carefully analyzed the relationship between battery voltage, performance, and power consumption in low battery conditions in which the operation scenario orchestrated by operating system (OS) is different from the case when the battery capacity has sufficient headroom. The main goals of the proposed sudden-voltage-drop-protection (SVDP) technique are rapidity, adaptivity, and low implementation cost.

2 Architecture and operation scenario of SVDP

Fig. 1 shows a typical power supply chain for an AP in a mobile device. The basic role of the PMIC is to provide a variety of stable operating voltages to the AP via a number of internal voltage regulators. Furthermore, the PMIC can adjust the voltage levels to maximize the energy efficiency based on the power management policy of the system. Additional power management can be performed using clock frequency control in the AP. Because each PLL occupies a large chip area, a wide range of clock frequencies is derived from PLLs by digital clock divider logic blocks to minimize the number of PLLs required.

Sudden voltage drops can occur when a mobile device abruptly enters a high performance mode, which draws large instantaneous current from the power supply. In this case, the PMIC usually sends a reset signal to AP in order to prevent system malfunction. Because we focus on prompt power adjustment under low battery conditions to cope with sudden voltage drops, the direct control of analog circuit components such as PLLs and voltage regulators, which require several milliseconds to stabilize, is not feasible. Therefore, we adopt an all-digital-
logic-based programmable control structure to meet the design objectives of rapidity, flexibility, and simplicity.

SVDP consists of two basic operations: voltage drop detection and AP clock frequency control. The hardware architecture of SVDP can be realized with four simple logic blocks: one comparator, one 2-to-1 multiplexer, and two registers, as shown in Fig. 2. SVDP operates in two steps, 1) sudden voltage drop detection by svdp_comparator and svdp_thr_register in the PMIC, 2) power consumption rate control via svdp_multiplexer and svdp_clk_div_register in the AP.

The PMIC asserts svd_warning_signal when a sudden voltage drop is detected by the voltage-level comparison between svdp_thr_register and the current battery voltage level. Accordingly, the CPU core clock frequency is reduced to the value of svdp_clk_div_register, thereby preventing reset or a halt. When svd_warning_signal is issued, the clock dividing ratio is set according to svdp_clk_div_register.

In this study, the starting point of low battery conditions is defined as 20 percent of the fully charged capacity of the battery, at which the power saving mode of most Android OS embedded products is initiated. The specifications of the reference Li-ion battery are as follows: the nominal (average) voltage is 3.85 V; the fully charged voltage level is 4.4 V; the full capacity is 3,220 mAh. Fig. 3 shows the expected effect of the SVDP near 3.52 V, which is the voltage level we consider to constitute low battery conditions. Sudden voltage drops around the UVLO threshold (in this case, 2.5 V) can be prevented by the SVDP technique (2 → 3 in Fig. 3). The voltage values in Fig. 3 depend on the battery specifications and system operation policies.

The bit-width of svdp_thr_register is determined experimentally to be 3 bits, which corresponds to 8-level control of the voltage range between 3.5 V and 2 V.
the UVLO threshold) for SVDP operation, which balances the power reduction ratio and the stability when changing the clock frequency. Additionally, we allocate 6 bits for svdp clk div register to be matched with the bit-width of clock divide value1, which is the other input to svdp multiplexer.

Fig. 2. Proposed SVDP architecture

Fig. 3. Idealized battery discharge curve for the SVDP technique under low battery conditions
In summary, the main role of the proposed technique is to reduce the rate of resets under low battery conditions using AP clock frequency control when entering the high performance mode. Possible scenarios are taking either bursts of still images or video recordings in an emergency.

### 3 Experimental results

We implemented the SVDP technique on a Samsung Exynos5433 AP and a PMIC product. Exynos5433 contains eight 64-bit ARM CPU cores, consisting of four Cortex-A57s and four Cortex-A53s fabricated in Samsung 20-nm CMOS process. This heterogeneous multi-core processing configuration for power reduction is called big.LITTLE [4]. The maximum operating clock frequencies of Cortex-A57 and Cortex-A53 cores are 1.9 GHz and 1.3 GHz, respectively, at 1 V, as shown in Fig. 4. The performance of a Cortex-A53 at its maximum operating clock frequency of 1.3 GHz is lower than that of a Cortex-A57 at 800 MHz, which is the minimum operating clock frequency of the Cortex-A57.

![Configuration of eight CPU cores and their operating clock frequency ranges within the AP](image)

To evaluate the SVDP technique, we used a two-phase test scenario for a basic zip-unzip test vector and capturing a burst of still images. Using the zip-unzip test vector is an easy method to induce repetitive instantaneous peak power mode, and thus, the expected SVDP effect can be observed with an oscilloscope. In addition, the battery output voltage recovery curve for different divided clock frequencies can be examined. The second phase of the experiment is performed for capturing a burst of still images to generate repetitive sudden voltage drop conditions and record the number of reset or halt occurrences.

The change of battery output voltage and CPU clock frequency under low battery conditions for the zip-unzip test vector are shown in Fig. 5 and Fig. 6, which were captured by a Tektronix DPO70404C oscilloscope.
As shown in Fig. 5, the PMIC issues \textit{svd\_warning\_signal} when the battery output voltage suddenly drops below the \textit{svd\_thr\_register} value of 3 V because of an instantaneous heavy load.

In Fig. 6, the \textit{svd\_clk\_div\_register} value for a Cortex-A57 was changed from 1.9 GHz to 0.95 GHz within 1 µs when entering the low battery condition, which is indicated by \textit{svd\_warning\_signal}. Because we use the clock divider logic for clock frequency control instead of using (time-consuming) PLL frequency control, half of the value of 1.9 GHz, i.e., 0.95 GHz, is selected. This value is the next largest clock frequency obtained using the digital clock divider logic.

As mentioned previously, SVDP does not perform direct control of voltage regulators or PLLs, which would incur a considerable cost in terms of timing and power consumption. Consequently, SVDP does not interfere with other implemented low-power techniques. The relationship between the battery voltage level
and the CPU clock dividing ratio is shown in Fig. 7. Fig. 7 indicates that as the value of the clock dividing ratio decreases, the speed of battery voltage recovery increases in an asymptotic manner.

![Battery voltage recovery curve for different clock dividing ratios](image)

Fig. 7. Battery voltage recovery curve for different clock dividing ratios

Furthermore, relative CPU core power consumption versus CPU clock dividing ratio is analyzed. Fig. 8 shows that the CPU power reduction effect is nearly saturated when the clock dividing ratio is lower than 1/6. This nonlinear behavior between the power consumption and the clock frequency can be explained by the increase in the fraction of the leakage power in total power consumption as the clock frequency increases. Although the leakage current is not directly related to the operating frequency, the increased temperature due to the high clock frequency contributes to an increase in the leakage term, as shown in Fig. 9, which was measured using an Exynos 5433 board. Based on these experimental data, SVDP can be adjusted to set an appropriate clock dividing ratio based on battery voltage and workload.

![CPU power reduction ratio](image)

Fig. 8. CPU core power consumption ratio versus clock dividing ratio
The final step is measuring the number of resets (or halts) under low battery conditions for system-level, real-world operation cases. We choose the capture of consecutive still images, which involves concurrent intensive operations among CPU cores, image signal processor (ISP), memory blocks, and on-chip interconnect networks. In this experiment, the number of consecutive still images captured is restricted to 10; otherwise, the reset cases due to continuous high power consumption could contaminate the evaluation results. The counts of failures are measured for 10 consecutive still images captured 100 times. As shown in Table I, we can completely eliminate the occurrence of resets.

### Table I. Failure rate comparison result

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<tr>
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<th>Without SVDP</th>
<th>With SVDP</th>
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<tbody>
<tr>
<td>Failure (reset or halt) rate</td>
<td>42/100</td>
<td>0</td>
</tr>
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</table>

Fig. 9. Leakage power to CPU core total power consumption ratio versus clock frequency

The final step is measuring the number of resets (or halts) under low battery conditions for system-level, real-world operation cases. We choose the capture of consecutive still images, which involves concurrent intensive operations among CPU cores, image signal processor (ISP), memory blocks, and on-chip interconnect networks. In this experiment, the number of consecutive still images captured is restricted to 10; otherwise, the reset cases due to continuous high power consumption could contaminate the evaluation results. The counts of failures are measured for 10 consecutive still images captured 100 times. As shown in Table I, we can completely eliminate the occurrence of resets.

#### 4 Conclusion

In this letter, we proposed an SVDP technique to minimize the occurrence of resets or halts when a mobile device enters high performance mode under low battery conditions. SVDP supports rapid AP power management to avoid system failure under low battery conditions and is cost-effective to implement. In addition, this method does not interfere with existing low-power management techniques.

The proposed SVDP technique is successfully implemented on one of the latest industrial products, i.e. Samsung Exynos5433 and an associated PMIC. The significance of this contribution can be summarized as extending the spectrum of power usage scenarios to enhance user satisfaction with mobile devices.
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