Impacts of flexible $V_{th}$ control, low process variability, and steep SS with low on-current of new structure transistors to ultra-low voltage designs

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Abstract: This paper discusses impacts of flexible $V_{th}$ control, low process variability, and steep SS with small on-current of new structure devices on ultra-low voltage circuits. Our simulation results based on PTM 22 nm model clarify applicability of ultra-low voltage operation to a nominal speed common SoC designs by an introduction of $V_{th}$ control as well as low power sensor nodes. We also reveal requirement of process variability suppression for high energy efficiency with steep SS transistors, and utilization of small on-current steep SS transistors to low power and low speed applications. Our qualitative discussion well explains these experiment results.

Keywords: process variability, adaptive body bias, ultra-low voltage circuits, energy efficiency

Classification: Integrated circuits

References

1 Introduction

The advancement of CMOS fabrication technology has brought various computer environments like high performance servers, personal computers, laptop or mobile terminals, and so on. Now, highly advanced CMOS technology gives us a prospect to computing nodes with ultra-low voltage operation and ultra-low power consumption. Current technology enables <10 ps single gate delay at about 1 V operation voltage, and even at an ultra-low voltage below 0.5 V, a few tens or hundreds KHz operation frequency is expected. In addition, though increase of circuit delay is in proportional to inverse of supply voltage $1/V$, computing energy per clock cycle is reduced in proportional to $V^2$. This high energy efficiency in the ultra-low voltage region gives a perspective to computing nodes with ultra-low power consumption. On the other hand, recent technology scaling is facing the limit of voltage scaling because of increasing the leakage current, and reduction of power consumption or raise of operation frequency by the scaling is limited in comparison with past processes. Recently, in addition to shrinking technology node, there are many proposals of new structure transistors which enable further advancement of LSI performance beyond the limit of the scaling, and such transistors are also considered to be more suitable for the ultra-low voltage operation.

Transistor called FD-SOI, ET-SOI, or SOTB [1, 2] was proposed as one of the improved structures of conventional planer bulk MOSFET. In this structure, pMOS and nMOS which have ultra-low dose channels are shaped on the thin SOI layer.
Ultra-low dose channel enables smaller random dopant variability of this SOI transistor in comparison with conventional MOSFET, and improvement of ultra-low voltage operation performance is expected. Another feature of this SOI transistor is flexible $V_{th}$ controllability by backgate biasing. Reference [1] reported that $V_{th}$ of SOTB transistor could be changed by over 0.3 V with backgate biasing. On the other hand, impact or effective utilization of $V_{th}$ control or small process variability on ultra-low voltage designs is scarcely discussed so far. A few works reported only experimental results of lowering operation voltage due to small process variability with SOTB [3, 4, 5].

Another approach is new structure transistors which enable steeper subthreshold slope (SS). Improvement of SS is effective for improving leakage current, and brings further benefits of scaling. FinFET is already in practical use, and achieved 75 mV/dec. SS [6]. The theoretical limit of SS of conventional CMOS at the room temperature is about 60 mV/dec., and Tunnel FET (TFET) is one of the candidates which overcome this limit [7, 8]. However, TFET is suffering from serious low on-current issue, and usefulness of TFET is currently unclear in spite of its sub-60 mV/dec. SS. Though there are several works about improvement of on-current of TFET [9], sub-60 mV/dec. SS was not achieved in such works.

In this paper, we discuss the impact of introduction of flexible $V_{th}$ control, improvement of SS and process variability, and utilization of low on-current steep SS transistors on ultra-low voltage designs based on simulations. Our contributions in this papers are following suggestions.

- Application of ultra-low voltage operation to common nominal speed SoCs by introduction of flexible $V_{th}$ control
- Requirement of process variability suppression for further advancement of ultra-low voltage designs
- Applicability of low on-current steep SS transistors to low speed applications

We first discuss the ultra-low voltage designs when flexible $V_{th}$ control is introduced based on simulations. Though ultra-low voltage designs have been considered to be applied to low speed applications, we suggest new application target of ultra-low voltage designs from discussions. In addition to flexible $V_{th}$ control, improvement of SS is also considered in simulations, and we clarify that reduction of the process variability will be required for obtaining high energy efficiency in ultra-low voltage designs with improved SS transistors. Finally, we investigate low on-current conditions of steep SS transistors like TFET, and we substantiate that low on-current steep SS transistors are useful for low power and low speed application even if their on-current is only 1/30–1/300 of that of planer MOSFETs.

In Sec. 2, we discuss impacts of the flexible $V_{th}$ control, process variability, and low on-current steep SS transistors on ultra-low voltage designs based on simulations. Section 3 describes theoretical discussions which explain the results obtained in Sec. 2, and Sec. 4 concludes this paper.
2 Simulation-based suggestions about new structure transistors in ultra-low voltage designs

2.1 Simulation setup

This section discusses the energy efficiency in ultra-low voltage designs with circuit simulations. We adopt Predictive Transistor Model (PTM) 22 nm LP [10] as a transistor model for simulations. The “NFACTOR” parameter of the BSIM4 [11] model is modified to adjust SS to about 80 mV/dec. 65 mV/dec. and 45 mV/dec. though original PTM model has about 100 mV/dec. SS. SmartSpice program [12] is adopted as a circuit simulator. “DELVTO” instance parameter of a transistor model implemented in SmartSpice simulator is exploited to change the \( V_{th} \) of transistors.

We simulated 29-stage inverter chain circuit. When we verify the impact of process variability, \( V_{th} \) of each transistor is varied randomly according to normal distribution, and average of simulation results of 34 chains is calculated. This simulation includes about 1000 gates, and impact of 3\( \sigma \) variations is expected to be observed. Both of rise-input and fall-input results are also simulated and averaged. When one or more chains failed to operate at the specific condition, the circuit operation is regarded to be failed at that condition.

2.2 Impact of introduction of \( V_{th} \) control to low-voltage design

As described in Sec. 1, new structure SOI transistors enable flexible \( V_{th} \) control by backgate biasing. This section discusses the impact of flexible \( V_{th} \) control on ultra-low voltage designs.

The introduction of \( V_{th} \) control changes the relation between power and delay in ultra-low voltage designs. Here, we simulate 100 mV/dec. transistor which is typical SS value of conventional planer Si MOSFET to obtain relation between power and delay. In ultra-low voltage designs, there is an inevitable tradeoff between a delay and a power. Power efficiency, i.e. energy/cycle, is improved by lowering of operation voltage instead of a larger delay. This relation can be drawn with a graph in Fig. 1(a) [13]. When the \( V_{th} \) control is introduced, the relation between the power, operation voltage, and \( V_{th} \) can be depicted with a contour map (dashed-line) in Fig. 1(b) [14, 15]. The 29-stage inverter delay is depicted with a
outside of the black solid line described with “Operation Limit” is the range where the circuit failed to operate. As observed on Fig. 1(b), $V_{dd}$ can be lowered with keeping circuit delay constant by flexible $V_{th}$ control. Fig. 2(a) depicts relation between energy/cycle and $V_{dd}$ when 29-stage inverter chain delay is kept 1 ns, 10 ns, 100 ns, 1 us, and 10 us. These delay contour lines are almost straight because the circuit delay is determined by $I_{on}$, and $I_{on}$ strongly depends on ($V_{dd}$ – $V_{th}$).

$V_{th}$ control enables lowering operation voltage and power consumption without compromising the delay, and even in a 1 ns delay with 29-stage inverter, energy/cycle is minimized at about 0.3 V. The minimum energy/cycle of larger ring period conditions are obtained in low voltage ranges. This result indicates that reduction of power consumption by lowering operating voltage is effective not only for ultra-low speed circuits like a sensor node, but also nominal speed circuits like common SoCs. In addition, further improvement of energy/cycle can be obtained with compromising the delay with $V_{th}$ control. Generally, the impact of leakage current for energy/cycle increases when the delay is increased. However, leakage current can be reduced by controlling $V_{th}$, and compromising the delay always improves energy/cycle when flexible $V_{th}$ control is introduced. This relation will be theoretically discussed in Sec. 3.

2.3 Lowering operation voltage and process variability when SS is improved

Figs. 2(a)–2(c) depict relation between energy/cycle and $V_{dd}$ when transistors have 100, 80, and 65 mV/dec. SS. Inverter chain delay is kept 1 ns, 10 ns, 100 ns, 1 us, and 10 us with $V_{th}$ control. When SS is improved, smaller energy/cycle is obtained, and minimum energy point (MEP) where minimum energy/cycle is obtained is shifted to a lower voltage. In case of SS = 65 mV/dec., MEP of inverter chain delay = 1 ns–10 us is about 0.24 V–0.13 V, and more efficient energy/cycle at MEP can be obtained in comparison with the case of SS = 100 mV/dec. Consequently, further lowering of operation voltage has the significant impact on improvement of energy/cycle when steeper SS transistors are introduced.

However, minimum operation voltage is limited by the process variability [13], and MEP is also obtained at a higher voltage when process variability increased.
Increase in leakage current or delay due to variability has a larger impact than decrease of them, and process variability increases energy/cycle. As distribution of $V_{th}$ variability is represented with normal distribution, transistors with $n_x$ ($n > 1$) current and with $1/n$ current equally likely appear in subthreshold operation. Here, increases in current and delay of circuits due to a pair of $n_x$- and $1/n_x$-current transistors can be represented as $(n + 1/n - 2)x = ((n - 1)^2/n)x$. This term indicates that increased process variability always worsens the energy/cycle. In addition, when circuits operate at near the minimum operation voltage, several cells which include large $V_{th}$ variation are nearly failing to operate, and these cells have an extremely large delay or current. As a result, energy/cycle is worsened near the minimum operation voltage, and MEP is obtained at a bit higher voltage than the minimum operation voltage.

Figs. 3 and 4 compare energy/cycle ($E/C$), supply voltage ($V_{ddopt}$), and threshold voltage ($V_{thopt}$) at MEP, $SS = 100 \text{ mV/dec.}$, $\sigma V_{th} = 0 \text{ mV}$, 20 mV, 40 mV, Delay = 1 ns–10 us.

Figs. 3 and 4 compare energy/cycle at MEP when the process variabilities $\sigma V_{th} = 0, 20,$ and 40 mV are given. Energy/cycle ($E_{C_{opt}}$), supply voltage ($V_{ddopt}$), and VTH0 ($V_{thopt}$) at MEP are depicted in Figs. 3 and 4. The minimum energy/cycle is deteriorated by process variability because higher operation voltage is required and $V_{ddopt}$ rises. When $SS = 100 \text{ mV/dec.}$, the minimum energy/cycles of $\sigma V_{th} = 0 \text{ mV}$ and 40 mV are 4.5–8.2 fJ (delay 1 ns–10 us) and 6.9–10.9 fJ, and impact of process variability is limited. However, in case of $SS = 65 \text{ mV/dec.}$, the minimum energy/cycles are deteriorated from 1.6–5.6 fJ to 4.3–8.0 fJ when $\sigma V_{th}$ is increased from 0 mV to 40 mV. The minimum energy/cycles in $SS = 65 \text{ mV/dec.}$, $\sigma V_{th} = 40 \text{ mV}$ case is nearly equal to $SS = 100$
mV/dec., $\sigma V_{th} = 0$ mV case, and improvement of SS is spoiled by the process variability. The MEP of SS = 65 mV/dec. case is lower than that of SS = 100 mV/dec. case, and the margin between minimum operation voltage and MEP is smaller in SS = 65 mV/dec. case. The impact of process variability gets more serious for ultra-low voltage operation when SS is improved. When $\sigma V_{th}$ is suppressed to 20 mV, minimum energy/cycle in SS = 65 mV/dec. is 2.1–5.8 fJ, which is not seriously degraded from SS = 65 mV/dec., $\sigma V_{th} = 0$ mV case. Suppression of variability is effective for improvement of energy/cycle in SS-improved transistors.

These results indicate that attractive high energy efficiency is obtained with steeper SS transistors at lower voltage than that of conventional SS transistors, and that sufficient suppression of process variability is also essential to obtain the benefits of these high energy efficiency with steeper SS transistors.

2.4 Utilization of small on-current sub-60 mV/dec. SS transistors in ultra-low speed application

TFET is one of the most prospective transistors which enable sub-60 mV/dec. SS. However, TFET is suffering from their small on-current. Here we clarify the required on-current for TFET based on simulation. We simulated SS = 45 mV/dec. transistor with smaller current which have 1/3, 1/10, 1/30, 1/100, and 1/300 on-current in comparison with nominal on-current of transistors in PTM 22 nm model. The mobility parameter of PTM model is modified to simulate small on-current.

Figs. 5(a) and 5(b) show the relation between energy/cycle and $V_{dd}$ when inverter chain delay is kept 1 ns and 100 ns respectively. When the inverter chain delay is 1 ns and circuit operates in nominal speed, even the 1/3 on-current spoil the impact of improvement of the SS, and 1/30, 1/100, and 1/300 on-current could not achieve 1 ns delay. However, in case of 100 ns delay which corresponds to subthreshold operation, even 1/30 on-current improved energy/cycle by about 20% at MEP in comparison with nominal on-current 65 nm/dec. transistor.

Fig. 5(c) depicts the simulated energy/cycle at MEP of nominal on-current 65 nm/dec. transistor, small on-current 45 nm/dec. transistors. Each of 1/10, 1/30, 1/100, and 1/300 small on-current 45 nm/dec. transistor achieved better energy/cycle than nominal on-current 65 nm/dec. transistor when inverter chain delay is
about over 10 ns, 30 ns, 100 ns, and 1 us respectively. We clearly observed that benefit of steeper SS can be obtained in subthreshold operation, and demonstrated that small on-current steep SS transistors are applicable to low-speed applications.

3 Qualitative discussions

This section describes qualitative discussions which supports discussions in Sec. 2 where we suggested application of ultra-low voltage design to nominal speed circuits, improvement of energy/cycle by compromising delay, effectiveness of lowering operation voltage and suppressing process variability with steeper SS transistors, and applicability of low on-current steep SS transistors.

Energy/cycle of \( n \) stage gates can be written as Eq. (1).

\[
EC \sim n \cdot C \cdot V_{dd}^2 + n \cdot V_{dd} \cdot I_{\text{leak}} \cdot D
\]

where \( EC \) is energy/cycle, \( C \) is the load capacitance, \( I_{\text{leak}} \) is the off-leakage current of the circuit, and \( D \) is delay of the circuit. The first and second terms of the right hand side are originated from the dynamic power and the static power respectively. The source-drain current in the subthreshold region can be written as Eq. (2) [11].

\[
I_{ds} = I_0 \cdot \left(1 - \exp\left(-\frac{V_{ds}}{v_t}\right)\right) \cdot \exp\left(\frac{V_{gs} - V_{th}}{n \cdot v_t}\right)
\]

where \( v_t \) is the thermal voltage. The constant \( I_0 \) determines \( I_{ds} \) at \( V_{gs} = 0 \). The off-leakage current can be calculated with \( V_{gs} = 0 \), \( V_{ds} = V_{dd} \) in Eq. 2. From Eq. (2), Eq. (1) can be approximated with Eq. (3) when \( V_{dd} > V_{th} \), that is, not in the subthreshold region. Delay \( D \) is in proportional to the time constant \( RC \) and the number of the stages of the circuit \( n \), and Eq. (3) is introduced as discussed in [16] when driver resistance \( R \) is substituted by \( V_{dd}/I_{\text{on}} \). The on-current \( I_{\text{on}} \) can be represented by common equation obtaining source-drain current of MOSFET in saturation region.

\[
EC \sim n \cdot C \cdot V_{dd}^2 + n^2 \cdot C \cdot I_0 \cdot \left(1 - \exp\left(-\frac{V_{dd}}{v_t}\right)\right) \cdot \exp\left(\frac{-V_{th}}{n \cdot v_t}\right) \cdot \exp\left(\frac{V_{dd}^2}{C_0 \cdot W (V_{dd} - V_{th})^2}\right)
\]

Delay \( D \) can be kept constant by lowering both of \( V_{dd} \) and \( V_{th} \). When \( V_{dd} \) and \( V_{th} \) are lowered, energy/cycle decreases according to Eqs. (1) and (3). This relation supports discussion about effectiveness of lowering \( V_{dd} \) and \( V_{th} \) at nominal speed for improvement of energy/cycle in Sec. 2.2. After \( V_{dd} \) and \( V_{th} \) is sufficiently lowered, increase of off-leakage current by \( \exp(-V_{th}) \) part become significant, and lowering \( V_{ds} \) with keeping the delay constant by \( V_{th} \) control increases energy/cycle. This increase of energy/cycle is also consistent with simulation results in Fig. 3(a).

We next focus on energy efficiency in subthreshold region. Assuming that \( I_{\text{on}} \) in the subthreshold region is current when \( V_{gs} = V_{ds} = V_{dd} \), relation between the \( I_{\text{on}} \) and off-leakage current in the subthreshold region is written as Eq. (4) [17].

\[
I_{\text{on}} = I_{\text{leak}} \cdot 10^{V_{dd}}
\]
where $S$ is the gradient of the SS (V/dec.). Equation (5) is obtained [18] from Eq. (1), Eq. (4) and $D \sim n \cdot C \cdot V_{on}/I_{on}$. Off-leakage current $I_{\text{leak}}$ and $V_{th}$ are dropped out in Eq. (5).

$$EC \sim n \cdot C \cdot V_{dd}^2 + n^2 \cdot V_{dd}^2 \cdot C \cdot 10^{-\frac{V_{th}}{S}}$$

(5)

Equations (3) and (5) indicate that by raising $V_{th}$, energy/cycle is improved in the above-threshold region and not improved in the subthreshold region. In near-threshold region, where circuit operation is shifted from above-threshold to subthreshold region, improvement of energy/cycle becomes slower when $V_{th}$ is raised. Consequently, in all of above-threshold, near-threshold, and subthreshold regions, raising $V_{th}$ does not increase energy/cycle. These relations are consistent with discussion about improvement of energy/cycle by raising $V_{th}$ and compromising delay in Sec. 2.2.

Equation (5) also indicates that static current is drastically reduced by improving the SS, and improvement of off-leakage current lowers MEP. Low operation voltage decreases dynamic current and better energy/cycle can be obtained at lower voltage with steeper SS transistors. Improvement of energy/cycle by the steeper SS, which was observed in Figs. 3 and 4 and discussed in Sec. 2.3, is consistent with Eq. (5).

We next discuss about the small on-current steep SS transistors. Here, we assume that on-current of the small on-current steep SS transistors, $I_{on}'$, is $1/m \cdot I_{on}$ with threshold voltage $V_{th}'$ at supply voltage $V_{dd}$ in comparison with common Si MOSFET with on-current $I_{on}$. When common MOSFET has sufficiently small $I_{on}$ in subthreshold operation, the threshold voltage of small on-current steep SS transistor $V_{th}'$ which satisfies $I_{on}' = I_{on}$ can be determined, and Eq. (6) is obtained.

$$\frac{1}{m} \cdot I_{\text{off}} \cdot 10^\frac{V_{th}-V_{th}'}{m} = I_{\text{off}} \cdot 10^\frac{V_{th}-V_{th}'}{m}$$

(6)

where $S_0$ and $S_1$ are SS gradient of common MOSFET and the small on-current steep SS transistor respectively. $I_{\text{off}}$ and $I_{\text{off}}'$ respectively determine $I_{on}$ at $V_{gs} = 0$ of common MOSFET and steep SS transistor. Off-leakage current of the steep SS transistor is represented as Eq. (7).

$$I_{\text{leak}}' = I_{\text{leak}} \cdot 10^\frac{V_{th}-V_{th}'}{m}$$

(7)

where $I_{\text{leak}}$ and $I_{\text{leak}}'$ are off-leakage currents of common MOSFET and the small on-current steep SS transistor. $I_{\text{leak}}'$ is smaller than $I_{\text{leak}}$ as long as $S_1$ is steeper than $S_0$. As $I_{on} = I_{on}'$ and $I_{\text{leak}} > I_{\text{leak}}'$, $EC_{\text{dyn0}}, EC_{\text{st0}}, EC_{\text{dyn1}}, EC_{\text{st1}}, EC_{\text{dynt0}}, EC_{\text{stt0}}, EC_{\text{dynt1}}, EC_{\text{stt1}}$, dynamic and static energies of $S_0$ and $S_1$ respectively, have relation in Eq. (7).

$$EC_{\text{dynt0}} = EC_{\text{dynt1}}, EC_{\text{stt0}} > EC_{\text{stt1}}$$

(8)

$S_1$ steeper SS and low on-current device achieves smaller energy/cycle because of smaller static energy in subthreshold operation when $V_{th}'$ adequately determined. Consequently, improvement of energy/cycle is expected with small $I_{on}$ steep SS transistors in low speed applications. These discussions well explain simulation results in Fig. 5 and discussions in Sec. 2.4.
4 Conclusion

In this paper, we discussed impacts of flexible $V_{th}$ controllability, low process variability, and steep SS with low on-current of new structure transistors on ultra-low voltage designs. Based on simulation, we clarified that when the flexible $V_{th}$ control is introduced, ultra-low voltage designs can be applicable to common SoCs as well as low speed applications. Operation voltage is increasingly lowered by development of steeper SS transistors, and reduction of process variability is also essential to utilize the ultra-low voltage region with high energy efficiency. Our experiments also indicated that small on-current steep SS transistors like TFETs, can be applicable to low power and low speed applications even if their on-current is 1/30–1/300 of common Si MOSFET.

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