A fully synthesizable injection-locked PLL with feedback current output DAC in 28 nm FDSOI

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Abstract: A feedback current output digital to analog converter (DAC) is proposed to improve the linearity of frequency and reduce the power consumption in this synthesized PLL. All circuit blocks are implemented with standard cells from digital library and place-and-routed automatically without any manual routing. The proposed PLL has been fabricated in a 28 nm fully depleted silicon on insulator (FDSOI) technology. The measurement results show that this synthesized injection-locked PLL consumes 1.4 mW from 1 V supply while achieving a figure of merit (FoM) of −235.0 dB with 1.5 ps RMS jitter at 1.6 GHz. This chip occupies only $64 \mu m \times 64 \mu m$ layout area with the advanced 28 nm FDSOI process. To the best knowledge of the authors, the PLL presented in this paper achieves the smallest area to date.

Keywords: standard cell, synthesizable PLL, low power, low jitter, small area, gated edge injection

Classification: Integrated circuits

References


1 Introduction

Due to highly-scaled CMOS IC technology, the analog circuits tend to be limited by the device gate leakage and low power supply. In order to take advantage of advanced technology, digitally-intensive and even all-digital circuits have been actively studied and become promising over traditional analog ones in terms of timing accuracy, power consumption and chip area [1, 2, 3, 4, 5].

PLL has been widely used as a critical component for clock generation and frequency synthesis in modern communication systems. While some fully synthesizable PLLs [2, 4] are published recently, their performances show some limitations in terms of large area and high power consumption. In addition, some custom-designed cells are utilized in these synthesized PLL, which result in degradation in terms of portability and scalability. To eliminate the custom-designed cells requiring manual placing and routing, a fully synthesizable phase-locked loop is proposed in [2] which is totally based on standard cells from digital library and automatically place-and-routed (P&R-ed) with commercial digital tools. However, this fully synthesizable PLL still costs a lot of power consumption due to a power-hungry DAC used for coarse tuning. Moreover, the linearity of conventional current output DAC is poor, which degrades the frequency linearity of phase coupled ring oscillator. In order to reduce the power consumption and improve the linearity of conventional DAC, a feedback current output DAC is proposed in this paper. This feedback DAC can lower the power consumption due to the decrease of $V_{GS}$ while providing a highly-linear frequency characteristics owing to the feedback property. Implemented in a 28 nm fully depleted silicon on insulator (FDSOI) process, the proposed fully synthesized PLL achieves an FoM of $-235.0$ dB with a power consumption of 1.4 mW from 1 V power supply and an area of only 0.004 mm$^2$.

This paper is organized as follows. Section II presents the system architecture. Section III explains the feedback current output DAC block. Experimental results of this synthesized PLL is described in Section IV. Finally, the conclusions are given in Section V.

2 System architecture

In a conventional synthesizable PLL [2], a current output DAC is composed of NAND gates, which is used for controlling a current starved ring oscillator.
However, this DAC design is power-hungry due to low impedance from power supply to ground. Considering that the NAND gates of conventional current output DAC mostly works as switches, it is clear that switches have low impedance so that the DAC power consumption is large. In addition, the DAC linearity is largely degraded because of tremendous changes in the operation region of transistors. Different from the conventional current output DAC, a feedback current output DAC is proposed in this paper to improve the frequency linearity while reducing the power consumption.

Fig. 1 shows the block diagram of the proposed synthesizable PLL with a feedback current output DAC. The digitized DCO frequency is compared with the predefined frequency control word (FCW) and the difference is then filtered by the digital loop filter (DLF) and then is used to adaptively tune the DCO frequency until frequency locked. Once the frequency locked loop set to a fixed frequency, the injection locking path is enabled and realizes the phase locking by the edge injection. The fully synthesized PLL entirely consists of digital standard cells and is place-and-routed without any custom design.

3 Feedback current output DAC

Fig. 2. Conceptual diagram of the conventional current output DAC.
For PLL design, there are some critical specifications, such as low power, small area, low jitter, wide tuning range and so on [6, 7, 8, 9, 10]. As proposed in our previous work [2], in order to realize a wide tuning range in synthesizable PLL, a current output DAC with the current starved ring oscillator is proposed which is shown in Fig. 2. If the control bit $D_N$ ($N = 0, 1, 2, 3$) is set to LOW, then the output becomes higher and if $D_N$ is set to HIGH, then the output becomes lower. Thus the transistors controlled by $D_N$ work in switched mode and can be equivalent to a voltage controlled variable current source.

However, the conventional synthesizable PLL [2] costs large power consumption for a given frequency tuning range due to poor frequency linearity. Thus the linearity of frequency controller becomes very critical if a wide frequency tuning range is required for a given power budget. In order to achieve required specification, a feedback current output DAC is proposed as shown in Fig. 3 and Fig. 4. Different from the conventional current output DAC, the proposed feedback current output DAC can achieve better linearity. If $D_N$ is set to LOW, then the output becomes higher and if $D_N$ is set to HIGH, then the output goes around $V_{DD}/2$ depending on voltage distribution. The detailed analysis about the difference between the conventional current output DAC and the proposed feedback current output DAC will be shown later.

Fig. 3. Conceptual diagram of the proposed feedback current output DAC.

Fig. 4. Schematic of the proposed feedback current output DAC.
In order to reduce the power consumption of conventional current output DAC, instead of using 2-input NAND gate, 3-input or even 4-input NAND gate is utilized as the unit cell which shows larger impedance from power supply to ground. As shown in Fig. 5, 3-input w/o feedback shows about 0.5 mW (25%) lower compared to 2-input w/o feedback one. However, the multi-input gate method is largely limited by process technology. In this paper, a feedback current output DAC is proposed to further reduce the power consumption of current output DAC. As shown in Fig. 3, the $V_{GS}$ of feedback PMOS cell is reduced to $V_{DD} - V_{OUT}$ while the conventional one is equal to $V_{DD}$ and the $V_{GS}$ of feedback NMOS is around $V_{OUT}$ while the conventional one is still equal to $V_{DD}$. According to the current equation of transistor, the smaller $V_{GS}$ is, the lower current it consumes for a fixed transistor.

Fig. 5 depicts that the proposed 3-input w/ feedback DAC consumes about 0.1 mW peak power while the 3-input w/o feedback costs 0.15 mW peak power. It is clear that proposed feedback DAC shows 30% reduction in peak power consumption compared with conventional one. In conclusion, for designing a low-power current output DAC based on standard cells, two effective ways are identified: one is to use multi-input NAND gates and the other is the proposed feedback current output DAC. To provide the proper current biasing for current starved ring oscillator, the MOSFETs for current controlling must work in saturation region to achieve current matching, namely $V_{GS} > V_{TH}$ and $V_{GS} - V_{TH} < V_{DS}$. The output voltage $V_{OUT}$ of the proposed feedback current output DAC must be above the threshold voltage $V_{TH}$ which is confirmed in Fig. 6.

As mentioned before, for a given power budget, high linearity is entirely required for frequency control once large tuning range is demanded. Fortunately, high linear frequency characteristics can be achieved by the proposed feedback current output DAC together with current starved ring oscillator. For the proposed feedback DAC, the transistors have two operating regions: NMOS saturation and PMOS linear, NMOS linear and PMOS linear. While the conventional one will have three operating regions, namely, from NMOS saturation and PMOS linear to...
Fig. 6. Simulated output voltage of the conventional current output DAC and the proposed feedback current output DAC.

Fig. 7. Operating region comparison and analysis of (a) the conventional current output DAC and (b) the proposed feedback current output DAC.

NMOS linear and PMOS linear, and then NMOS linear and PMOS saturation. Fig. 7 provides the operating region comparison and analysis of conventional current output DAC and proposed feedback current output DAC. The proposed feedback DAC almost operates in the same region, namely, NMOS saturation and PMOS linear, so it is clear that proposed DAC can provide better linearity compared to the conventional one. The two operating regions of the proposed
feedback current output DAC can be expressed approximately by the following two simplified current equations:

\[ N_n \beta_n \left( V_{GSN} - V_{THN} \right)^2 = N_p \beta_p \left( V_{GSP} - V_{THP} \right) V_{DSP} - \frac{V_{DSP}^2}{2} \]  \hspace{1cm} (1)

\[ N_n \beta_n \left( V_{GSN} - V_{THN} \right) V_{DSN} - \frac{V_{DSN}^2}{2} = N_n \beta_n \left( V_{GSP} - V_{THN} \right) V_{DSN} - \frac{V_{DSN}^2}{2} \]  \hspace{1cm} (2)

Fig. 8. Frequency linearity comparison of the conventional current output DAC, the proposed feedback current output DAC and the measurement result.

Fig. 9. Frequency DNL comparison.

The three operating regions of the conventional current output DAC can be given as below:

\[ N_n \beta_n \left( V_{GSN} - V_{THN} \right)^2 = N_p \beta_p \left( V_{GSP} - V_{THP} \right) V_{DSP} - \frac{V_{DSP}^2}{2} \]  \hspace{1cm} (3)

\[ N_n \beta_n \left( V_{GSN} - V_{THN} \right) V_{DSN} - \frac{V_{DSN}^2}{2} = N_p \beta_p \left( V_{GSP} - V_{THP} \right) V_{DSP} - \frac{V_{DSP}^2}{2} \]  \hspace{1cm} (4)
\[
N_n \beta_n \left( (V_{GSN} - V_{THN}) V_{DSN} - \frac{V_{DSN}^2}{2} \right) = N_p \beta_p \left( (V_{GSP} - V_{THP})^2 \right).
\]

where \( N_n \) stands for the number of NMOS transistors, \( N_p \) stands for the number of PMOS transistors, \( \beta_n \) is equal to \( \mu_n C_{ox} \frac{W}{L_n} \), \( \beta_p \) is equal to \( \mu_p C_{ox} \frac{W}{L_p} \). Please note that to simplify the equation, all the parameters used here are the absolute value of them.

To verify whether the frequency linearity is improved or not, simulated frequency and measured frequency versus digital control code are shown in Fig. 8. In order to clearly quantify the linearity, Fig. 9 shows the simulated differential nonlinearity (DNL). The DNL of simulation with conventional DAC ranges from \(-0.44\) to \(0.81\) LSB while the simulation with proposed DAC ranges from \(-0.59\) to \(0.44\) LSB and the measured DNL ranges from \(-0.23\) to \(0.47\) LSB. Thus, the oscillator using a feedback DAC shows better linearity compared to the one using the conventional DAC. As shown in Fig. 8, measurement frequency is several hundred MHz lower than simulated frequency with proposed DAC due to parasitic capacitors and resistors of placement and routing. In conclusion, the proposed feedback current output DAC achieves three key characteristics: 1) lower power consumption, 2) \( V_{OUT} \) is always above \( V_{TH} \), 3) higher frequency linearity.

### 4 Edge injection realization

In the conventional injection locking PLL, pulse injection [8, 9] is utilized frequently while pulse width calibration is always adopted to reduce the reference spur. Fig. 10 shows the edge injection realization schematic.

The reference is delayed by digitally-controlled delay line before passing the control logic and timing logic. As shown in the time domain figure, the output of timing logic gives the tunable injection window and injection edge signal [2]. When injection window is HIGH, the output of the inverter is LOW, which makes the \( V_X \) equal to 1. At this moment, the phase coupled ring oscillator is disable by pulse window and edge signal is enable to be injected to the oscillator and replace the initial oscillating edge at the output \( V_Y \).

![Fig. 10. Block diagram of edge injection.](image)
5 Measurement results

The proposed fully synthesizable PLL is designed and implemented in a 28 nm FDSOI technology. Fig. 11 shows a micrograph of the PLL which only occupies an area of 64 μm × 64 μm. As indicated in the die micrograph, PLL drawn in the black rectangular takes only part of the whole chip and the layout detail is depicted in the right part. The phase noise characteristic is evaluated by using a signal source analyzer (Agilent E5052B) and the spectrum is measured by using a spectrum analyzer (Agilent E4407B). Fig. 12 shows the measured phase noise with 1 V supply. Due to noise shaping characteristic of injection locking, the phase noise of injection locked PLL shows large improvement compared with free running. The phase noise maps to a 1.5 ps integrated jitter (from 1 kHz to 10 MHz).

At a 1.6 GHz output frequency, the power consumption is 1.4 mW excluding output buffers leading to an FoM of −235.0 dB, where FoM is defined as $10 \log \left( \frac{\gamma^2}{P_{\text{out}}(1\text{mW})} \right)$. Fig. 13 shows the measured spectrum with 1st order reference spur around −39 dBc where the injection frequency is 400 MHz.

Table I draws a result comparison between synthesized PLLs of recently published papers [2, 4] and that of this study. The proposed PLL with feedback current output DAC consumes lower power consumption than the conventional
### Table I. Performance comparison with state-of-the-art synthesized PLLs.

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**Fig. 13.** Measured spectrum.

**Fig. 14.** FoM comparison with state-of-the-art PLLs.
PLL leading to 0.6 dB improvement in FoM. Due to the linearity improvement of the feedback current output DAC, the DNL of the proposed PLL is only half of the conventional PLL.

Fig. 14 depicts a comparison between the previous works and the proposed PLLs in terms of FoM versus area. As shown in Fig. 14, the proposed injection locked PLL achieves better FoM due to lower power consumption DAC while occupies a smaller area.

6 Conclusion

A compact and low-power fully synthesized PLL using feedback current output DAC is presented. All building blocks are implemented with standard cells from digital library and place-and-routed automatically without any manual routing. The proposed PLL is fabricated in a 28 nm FDSoI technology and achieves an FoM of $-235.0$ dB with 1.4 mW power consumption from 1 V supply while occupies the smallest area (0.004 mm$^2$) to date with 28 nm FDSoI process. The proposed feedback current output consumes lower power consumption while improving the frequency linearity.

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