A novel SEU tolerant SRAM data cell design

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Abstract: An improved SEU tolerant SRAM data cell design is presented here. The cell enhances the capability of SEU tolerance by creating spatial redundancy of data and virtue of latch design. The results show that our proposed design achieves high resilience to SEU and provides a 300 times increase in critical charge compared to standard 6T cell without much degradation in speed and Power dissipation. It shows that our design is very suitable for applying in high-reliability circuit and system design.

Keywords: single event upset, radiation-hardened SRAM

Classification: Integrated circuits

References


1 Introduction

Significant improvements in performance have been brought about by CMOS downscaling. However, it has also introduced reliability concerns for circuit designers. For lacking of mask mechanism like combinational logic circuit, Data Cells like static random access memories (SRAM) and latches are extremely
susceptible to radiation strikes, such as cosmic rays, alpha particles and protons. When these particles strike the sensitive nodes of the memories, charge is injected into the diffusion regions, causing a voltage fluctuation which is called transient fault (TF) [1]. If the injected charge exceeds the Critical charge (Qcrit), upset event may occur, generally known as Single event upset (SEU) or soft error.

Compared to circuit-level design, system-level design seems to be a costlier option in terms of area, power and delay. As a result, circuit level design seems to be a more attractive way for reliable researchers. During the past 30 years, dozens of novel SEU robust SRAM cells have been proposed and obvious improvement in critical charge have been achieved [2, 3, 4, 5]. ROCK cell [2] can be regarded as a marvelous SEU Tolerant SRAM cell design. Six transistors P1–P6 are added to the standard 6T cell as shown in Fig. 1(a), the additional PMOS transistors have to be sized as ‘strong transistors’ to restore the value destroyed by SEU through the virtue of latch design. 10T cell proposed in [3] (Fig. 1(b)) and 12T in [4] (Fig. 1(c)) achieve their SEU tolerance by inserting pairs of transistors operating in linear region. The additional transistors work as resistors to block the feedback path and create spatial redundancy of data. These designs are quiet economical in terms of transistors and area overhead. However, two pairs of access transistors are needed to help write response, which makes the capacitive load of the bit line doubled, resulting more power dissipation for the chip. A quad-node 10-T soft robust SRAM cell named as Quatro-10T was proposed in [5], the cell exhibits larger noise margin in sub-0.45 V regime and less leakage current than DICE cell [6]. As a result, Quatro-10T cell seems more attractive in low voltage circuit designs. However, some inner nodes of this cell are not robust enough and its critical charge of these nodes is only 3 times more than standard 6T cell.

In this paper, a novel robust SRAM cell is proposed. By creating spatial redundancy of data and virtue of latch design, the cell achieves high reliability to SEU without much compromising on performance.

2 Proposed SEU robust cell design

The proposed SEU hardened SRAM cell design is shown in Fig. 1(d). On the basis of standard 6T SRAM cell, we added additional transistors N3, N4, P3 and P4 whose gates are connected with supply voltage or ground. These transistors operating on linear region create spatial redundancy of data. Additionally, transistors P5, P6, N5 and N6 are added to form the virtue of latch design as cell proposed in [7], which help storage nodes recover to their original value once the inner node is hit by SEU.

First, we have to check the write and read activity of the proposed cell. During write operation, Bit lines (BL and BLB) are driven to the opposite logic value by the write circuit block. When CLOCK signal (WL) is active, BL pull up/down the potential at storage node B and BLB pull down/up the potential at node A. New value is written into the storage node immediately by the positive feedback structure of the data cell. During read operation, Bit lines are pulled up to high potential by the pre-charge circuit block. When the rising edge of Clock signal comes, the driven transistors N1 and N3 charge/discharge BL/BLb if \( VA = 0/1 \).
Small voltage difference occurs between the bit lines, which will be captured by the sense amplifier and read out.

Assuming that the value “1” are written to node A, after the write process, the values at nodes A/B, C/D and E/F are 1/0, 1/0 and 1/0. We study the behavior of these inner nodes during a TF and show how the effects are mitigated in the proposed design. Firstly, we have to explain the conception of the sensitive node. When a NMOS stores logic ‘1’, it is susceptible to SEU, because the body voltage is 0 and the drain is at logic ‘1’, negative charge will inject to the drain if a ion strikes the device, causing drain voltage go to logic ‘0’. As for a PMOS, it can safely store logic ‘1’ while susceptible to SEU when stores ‘0’. After write response, we can find that node A, B, C and F are those sensitive nodes.

Case 1-vulnerability of node A, Node A is vulnerable when the drain of the transistor N6 is struck, the excess charge will cause node A to go low, since N3 is operating on linear region, node C has the potential to go low, momentarily turning transistor N2, N6 off. Nodes D and B keep stable since no charge of stored data is involved. Node E has the potential to go low too, but transistor P1 has max drive strength than P2, node E remains logic “1”. Node Q eventually recovers to high through P6 (on).

Case 2-vulnerability of node B, Node B is vulnerable if the drain of transistor P5/N5 is struck. The situation is similar to the previous case, the excess charge cause node B and node F to go high, then transistors P1 and P6 turn off, since node A and E is at high impedance state, no charge of stored data state at node A and E is involved. Node B recovers to low state through transistor N5 (on).
Case 3-vulnerability of node C, Node C is prone to SEU when ions strike the drain of transistor N2. Then node C goes low and turns the transistors N4 and N5 off. However, no charge at Node B and F is involved, Transistor N3 (on) pulls N up to the original high state.

Case 4-vulnerability of node F, Node F is vulnerable if the drain of transistor P3 is struck. The situation is similar to Case 3. It goes to high state due to the SEU and turns the P1 and P6 off. Values at Node A and C keep stable. Since the transistor N2 has max drive strength than N4. Node F is eventually recharged to low due to P4 (on).

3 Simulation results analysis and discussion

In order to simulate the particle injection, an exponential current pulse as below is used to determine the critical charge with the simulation tool Cadence Spectre. The critical charge required for a soft-error of each internal node can be figured out by iteratively increasing the injected charge by a small amount. The write time is defined as the time interval from the midpoint of the rising edge of an activated clock pulse to the midpoint of rising or falling edge of the response of the storage node.

The response for the standard 6T cell is shown in Fig. 2(a) when a $0 \rightarrow 1$ TF hit the node B at hold time (17 ns), the logic values flipped when the charge injected is 10 fC. Large voltage fluctuation occurs at node B, resulting in pulling down the value at node A.

Fig. 2(b) illustrates a recovery procedure of the proposed design when it is subjected to a $0 \rightarrow 1$ TF at node B with 200 fC injected charge. Even though the voltage fluctuation at node B is over 2 V, the value at node B recovers to its original state within 1 ns.

Similarly, a large $1 \rightarrow 0$ TF with 200 fC injected charge at node A can be mitigated as shown in Fig. 2(C). By increasing the injected charge until the cell flipped, we find that the critical charge of this design can be up to 3.48 pC, 366 times more than that of standard 6-T cell, as a consequence, the proposed design is an extremely robust design for inner nodes.

The performance of the proposed design is compared with previous robustness cells proposed in [2, 3, 4, 5]. The comparative parameters include transistor number, Qcrit, write time, power dissipation, leakage current, power delay product (PDP) penalty and area penalty. For fair comparison, we simulate all designs using Cadence Spectre and 65 nm model files of TSMC at 1.2 V supply voltage at 27°C temperature with a frequency of 100 MHz while no additional capacitive load is added. The simulation results are given in Table I.

Among all of the robust cells, the proposed cell has the largest transistor number, but not the largest area penalty because the design has no restrict requirement on transistor size as ROCK cell. The robust cell in [3] and [4] features perfect power dissipation, however, as pointed before, the additional pair of access transistors will introduce more capacitive load to bit line and word line, resulting much more additional power in the whole SRAM chip. The proposed cell has the equivalent write speed and PDP penalty to that of other cells, while the PDP penalty can be calculated as:
The leakage current is prominent, which means that the design is more attractive in advanced technology. The most remarkable point is that the cell has amazing critical charge. By creating spatial redundancy of data and virtue of latch

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PDP_{\text{penalty}} = \frac{PDP(\text{robust\_cell}) - PDP(\text{Standard\_6T\_cell})}{PDP(\text{Standard\_6T\_cell})} \quad (1)
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**Fig. 2.** Hold time when subjected to TF at 17 ns. (a) Voltage response when a 0 → 1 TF with 10 fC charge strike the node B of standard 6T cell. (b) Voltage response when a 0 → 1 TF with 200 fC charge strike the node B of proposed cell. (c) Voltage response when a 1 → 0 TF with 200 fC charge strike the node A of proposed cell.
design, the cell is robust to SEU with critical charge more than 300 times of that of standard 6T cell. Addition to SRAM cells, our proposed design can be used for robust data latches in logic circuit designs. The data latches are often used in latch chains and as separate logic gates for data manipulation and storage [8].

4 Conclusion

In this paper, we proposed an improved radiation hardened SRAM design. Simulation results show that the design achieves high resilience to SEU with the amount of critical charge at least 300 times more than that of standard 6-T cell. Compared to previous SEU robust designs, the proposed cell has less compromising on performance in terms of speed and power dissipation.

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