Study on thermal stress and keep-out zone induced by Cu and SiO$_2$ filled coaxial-annular through-silicon via

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Abstract: Coaxial-annular through-silicon via (CA-TSV) is a novel TSV structure. In this letter, the thermal stress and keep-out zone (KOZ) of Cu and SiO$_2$ filled CA-TSV are studied, considering anisotropic property of silicon. Firstly, by employing ANSYS software, the CA-TSV-induced thermal stress is simulated and analyzed. Secondly, by evaluating the effects of thermal stress on carrier mobilities of pMOS and nMOS channels, the KOZs induced by CA-TSV is estimated and compared with those of coaxial TSV (C-TSV), for the cases of transistor channels along [100] and [110] orientations. It is proved quantitatively that CA-TSV has better thermo-mechanical performance than C-TSV.

Keywords: thermal stress, keep-out zone (KOZ), anisotropic silicon, coaxial-annular through-silicon via (CA-TSV)

Classification: Integrated circuits

References

1 Introduction

By allowing heterogeneous integration of chips associated with high-speed interconnections, the three-dimensional integrated circuit (3D IC) has attracted tremendous interest in semiconductor industry [1]. For that purpose, the key technology enabler is the through-silicon via (TSV), which consists in a metal vertical interconnection crossing the silicon substrate [2]. By utilizing TSV in 3D IC, the average and the maximum distance among components on different dies will be substantially reduced, decreasing delay, power, and area factors [3]. Cu and SiO2 are widely used as TSV metal and dielectric materials, respectively [4]. However, when the TSV-based 3D IC is subjected a thermal ramp in the process flow, the TSV induces thermal stress in the silicon substrate, owing to the mismatch in coefficient of thermal expansion (CTE) between Cu (18 ppm/°C) and silicon (2.3 ppm/°C) [5, 6]. And then, the carrier mobilities of pMOS and nMOS transistor channels would be affected. Keep-out zone (KOZ) is a common quantitative representation for the impact of thermal stress on transistors [7].

Recently, coaxial-annular TSV (CA-TSV) is proposed to decrease the KOZ induced by coaxial TSV (C-TSV) [8]. However, the silicon substrate is simplified as a kind of isotropic material in Ref. [8]. In fact, the anisotropy of silicon has significant impact on KOZ, which is very different from the isotropic case [9]. There are no reports on the thermal stress and KOZ induced by CA-TSV and on its superior thermo-mechanical performance over C-TSV, with consideration of the anisotropic property of silicon. Therefore, it is necessary to investigate those aspects in detail. In this letter, the thermal stress induced by Cu and SiO2 filled CA-TSV are studied. The KOZs of CA-TSV are calculated and compared with those of C-TSV.

2 Thermal stress analysis

The geometry of CA-TSV is shown in Fig. 1(a). A CA-TSV is composed of a center SiO2 cylinder, two Cu annuluses nested coaxially and separated by a SiO2 annulus, and an outer SiO2 liner to separate Cu from silicon substrate. For comparison, Fig. 1(b) gives the structure schematic of C-TSV, which is composed of a Cu core, surrounding SiO2 and Cu annuluses, and an outer SiO2 liner. According to the current technology, the structure parameters of CA-TSV and C-TSV are set as follows: TSV height is 50 µm; both annular Cu thickness tm and annular SiO2 thickness td are 1 µm; cylindrical SiO2 diameter rd is 2 µm; cylindrical Cu diameter rm is 3 µm; and outer SiO2 liner thickness is 0.1 µm.

In order to investigate the performance of CA-TSV-induced thermal stress, finite element analysis (FEA) simulation is performed by employing ANSYS software [10]. Fig. 2 shows the geometry and mesh of finite element axisym-
ometric model for the TSV induced stress calculation. For symmetry, only one-eighth of the structure is used in the FEA simulation. Frictionless support is used for the left, right, and bottom cross sections. Hex dominant meshing method is selected for simulations. The contact element size of the TSV and substrate contact face is set as 0.1 µm, and the mesh element sizes of TSV and substrate are 0.5 and 1 µm, respectively. The radius of silicon substrate is 55 µm. There are a total of 4411714 nodes and 1066901 elements in the model. In the simulation, the anisotropic property of silicon and elasto-plastic property of Cu are taken into account, and SiO₂ is treated to be linear elastic. The temperature ramp is $-250°C$ [9].

The most common case is investigated that transistors are placed with the channel aligned along [100] and [110] crystal direction on (100) silicon wafer. Two kinds of situations are studied in this work. One is that the transistor is at $x$-location; the other is that the transistor is at $y$-location, as shown in Fig. 3.

Fig. 4 summarizes the FEA results of CA-TSV-induced thermal stress. Fig. 4(a) and (b) display the profiles of thermal stress components in $x$-direction ($\sigma_x$) and that in $y$-direction ($\sigma_y$), respectively, for [100] channel orientation (the case of Fig. 3(a)). Fig. 4(c) and (d) exhibit those for [110] channel orientation (the case
of Fig. 3(b)). Fig. 4 demonstrates that, significant stress (as much as \(\sim 400\) MPa) has been induced in silicon around CA-TSV. As shown in Fig. 4(a) and (b), or Fig. 4(c) and (d), the stress components in \(x\)-direction and \(y\)-direction have approximately inverse values because of the symmetry of the structure.

![Diagram](image)

**Fig. 3.** Transistor location and channel orientation in the proximity of TSV. Transistors are placed with the channels aligned along (a) [100] and (b) [110] crystal directions.
KOZ evaluation and discussion

Keep-out zone (KOZ) is a common quantitative representation for the impact of thermal stress on transistors, meaning the region where the transistors cannot be placed, as shown in Fig. 3. In this section, CA-TSV-induced KOZs are investigated. KOZ can be defined as the region surrounding TSV within which the variations of carrier mobility ($\Delta \mu / \mu$) are over 5% [11]

\[
\begin{align*}
\text{KOZ}_x\text{-location} &= x \left| \frac{\partial \Pi}{\partial \sigma_x} \right| > 5\% = x \left| \Pi_1 \sigma_x + \Pi_2 \sigma_y \right| > 5\% \\
\text{KOZ}_y\text{-location} &= y \left| \frac{\partial \Pi}{\partial \sigma_y} \right| > 5\% = y \left| \Pi_1 \sigma_y + \Pi_2 \sigma_x \right| > 5\%
\end{align*}
\]

where $\Pi$ represents piezoresistance coefficient, and $\sigma$ is the thermal stress. For [100] channel orientation, $\Pi_1$ and $\Pi_2$ are $-1.022 \times 10^{-3}$ and $5.37 \times 10^{-4}$ MPa$^{-1}$ for nMOS transistor, respectively, and $6.6 \times 10^{-5}$ and $-1.1 \times 10^{-5}$ MPa$^{-1}$ for pMOS transistor, respectively. For [110] channel orientation, $\Pi_1$ and $\Pi_2$ are $-3.16 \times 10^{-4}$ and $-1.76 \times 10^{-4}$ MPa$^{-1}$ for nMOS transistor, respectively, and $7.18 \times 10^{-4}$ and $-6.63 \times 10^{-4}$ MPa$^{-1}$ for pMOS transistor, respectively.

Fig. 4. Profiles of thermal stress components on the surface of silicon substrate. Profiles of (a) stress component in $x$-direction ($\sigma_x$) and (b) in $y$-direction ($\sigma_y$) for [100] channel orientation, and (c) that in $x$-direction ($\sigma_x$) and (d) that in $y$-direction ($\sigma_y$) for [110] channel orientation. The unit is MPa.

Fig. 5. KOZs induced by CA-TSV and C-TSV for nMOS and pMOS of different locations and channel orientations. The transistors are placed with the channel aligned along (a) [100] and (b) [110] crystal direction.
According to the thermal stress results in Fig. 4 and Eqs. (1) and (2), the KOZs in $x$- and $y$-direction are evaluated and compared with those of C-TSV [9], as shown in Fig. 5. It is shown that, for pMOS of [100] channel orientation, there is no KOZ induced by CA-TSV and C-TSV; for nMOS of [110] channel orientation, the KOZs induced by CA-TSV and C-TSV are negligible. In addition, for [100] channel orientation, the KOZ induced by CA-TSV decreased $2.2 \mu m$ (14.1%) compared with that of C-TSV for nMOS at $x$-location, and $2.8 \mu m$ (17.6%) for nMOS at $y$-location. For [110] channel orientation, the KOZ induced by CA-TSV decreased $3.1 \mu m$ (24.4%) compared with that of C-TSV for pMOS at $x$-location, and $3.3 \mu m$ (25.0%) for pMOS at $y$-location. Therefore, it is proved that CA-TSV has better thermo-mechanical performance than C-TSV with consideration of anisotropic property of silicon.

4 Conclusion

In this letter, the thermo-mechanical performance of Cu and SiO$_2$ filled CA-TSV is investigated with consideration of anisotropic property of silicon. Firstly, the thermal stress induced by CA-TSV is studied by employing ANSYS. Secondly, the CA-TSV-induced KOZs are calculated, and a comparison is made between the KOZs induced by CA-TSV and C-TSV. It is shown that there are hardly any KOZs induced by CA-TSV and C-TSV for pMOS of [100] channel orientation and nMOS of [110] channel orientation. And for pMOS of [110] channel orientation and nMOS of [100] channel orientation, the KOZ induced by CA-TSV decreased 2.2~3.3 $\mu m$ (14.1~25.0%) compared with that of C-TSV. Therefore, it is proved that CA-TSV has better thermo-mechanical performance than C-TSV as anisotropic property of silicon is taken into account.

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