Bootstrapped ring oscillator with feedforward inputs for ultra-low-voltage application

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Abstract: A novel ring oscillator is proposed for ultra-low-voltage application. The proposed ring oscillator utilizes the voltage bootstrapping to enhance the oscillation speed at near- and sub-threshold voltage regions. The delay cell for the proposed oscillator is configured with feedforward inputs coming from multiple previous stages for further enhancing the speed with low power consumption. The proposed ring oscillator was designed in a 65-nm CMOS process. Evaluation results indicate that the proposed delay cell has up to 50.8% lower latency with up to 23.5% less power consumption for the supply voltage ranging from 0.35 V to 0.6 V. They also indicated that the oscillation frequency of the proposed ring oscillator was improved by 44.5%~103.3% as compared to the conventional bootstrapped ring oscillator. For providing the same oscillation frequency, the proposed ring oscillator has 22.6% less power consumption.

Keywords: ring oscillator, VCO, bootstrapping

Classification: Integrated circuits

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1 Introduction

Ring oscillators (ROs) are important circuit elements in analog and digital IC designs. They have long been used for the design of phase-locked-loops (PLLs), analog-to-digital converters (ADCs), frequency synthesizers, and high-speed clocking subsystems [1, 2, 3, 4, 5, 6]. Nowadays, as the supply voltage of modern ICs is scaled down toward the near- or sub-threshold region, ring oscillators reliably operating in this region are required [7, 8]. However, unfortunately, as the supply voltage is scaled down, the oscillation speed of a ring oscillator is exponentially degraded and its linearity cannot be maintained. Also, the oscillation frequency change caused by process variations becomes serious. One solution for addressing these issues is to use the voltage bootstrapping technique [9], in which some internal node voltages along the timing-critical signal paths are boosted above the supply voltage or below the ground to enhance device strengths. Recently, a ring oscillator based on this technique was suggested [10]. However, the oscillation frequency of the ring oscillator is still not high, letting it be unsuitable for high-speed applications. To address this issue, a novel bootstrapped ring oscillator operating at ultra-low voltage region with higher oscillation frequency has been proposed. In Section 2, the conventional bootstrapped ring oscillator is explained and its limitations are described. In Section 3, the proposed bootstrapped ring oscillator is introduced and its operation is described with advantages. Comparison results are described in Section 4. The conclusions are then given in Section 5.

2 Conventional bootstrapped ring oscillator

The conventional bootstrapped ring oscillator is depicted in Fig. 1 [10], where the unit delay cell is shown in Fig. 1(a) and an N-stage implementation is shown in Fig. 1(b). The delay cell consists of a pair of input inverters (MP3/MN3 and MP4/MN4), boosting capacitors (C_{PU} and C_{PD}), precharge transistors (MP1 and MN1), and driver transistors (MP2 and MN2). When input A is high and Y is low (Y is actually below the ground as seen shortly later), $BA1$ is set to be low by MN3 and PU is precharged to be high by MP1. When A transitions to be low, $BA1$ is pulled up, letting PU be boosted above V_{DD} by the capacitive coupling through C_{PU} . Then, by an enhanced driving capability of MP2, Y is fast pulled up to the boosted voltage level. At the same time, $BA2$ is set to be high by MP4 and PD is precharged to be low by MN1. When A transitions to be high, $BA2$ is pulled down, letting PD be boosted below the ground by the capacitive coupling through C_{PD} . Then, by an enhanced driving capability of MN2, Y is fast pulled down to the negative boosted voltage level. Although the conventional ring oscillator can attain an increased oscillation frequency by taking advantage of voltage bootstrapping, the speed gain is not as much as expected since the critical path established is not just through a

Fig. 1. Conventional bootstrapped ring oscillator [10]: (a) unit delay cell structure, (b) N-stage implementation

driver transistor but through an input inverter, a boosting capacitor, and a driver transistor. Moreover, for taking full advantage of voltage bootstrapping, the up-boosting (down-boosting) transition of PU (PD) at the source of MP2 (MN2) must be slightly earlier than the falling (rising) transition of A at the gate of MP2 (MN2). But, since a boosting operation is initiated by an input transition, the boosting transition always occurs later than the associated input transition after the latency of the boosting signal path. This sort of timing mismatch can cause a lower boosted voltage, resulting in further degradation of speed and increase of power consumption. Additionally, since the on/off control of precharge transistors is done by the output, the turn-off of them is done only when the output has a sufficient voltage transition after the activation of the boosting operation, letting some boosted charge be lost through precharge transistors. In the next section, we present a new bootstrapped ring oscillator to provide a higher oscillation frequency by letting the boosting operation be initiated at an earlier timing and by overcoming the bootstrap timing mismatch.

3 Proposed bootstrapped ring oscillator

The proposed bootstrapped ring oscillator is depicted in Fig. 2, where the unit delay cell is shown in Fig. 2(a) and an N-stage implementation is shown in Fig. 2(b). The structure of the proposed delay cell is the same as that of the conventional except for the connection of some inputs. Whereas driver transistors MP2 and MN2 are driven by main input *A* coming from the first previous stage, the input inverters driving the boosting capacitors are driven by a feedforward input *PPA* coming from the third previous stage to allow an earlier start of boosting operations. Precharge transistors MP1 and MN1 are also driven by another feedforward input *PA* coming from the second previous stage to prevent charge loss, which was the problem in the conventional structure. When inputs *PPA* and *PA* are high and low, *BPPA1* and *PU* are precharged to be low (by MN3) and high (by MP1). When *PPA* falls and *PA* rises, *BPPA1* is pulled up and MP1 is turned off. Then, *PU* is boosted above VDD by a capacitive coupling by C_{PU} , resulting in an increased driving strength of MP2 to speed up the pull up transition of the output. During this time, *BPPA2* and *PD* are precharged to be high (by MP4) and low (by MN1). When input *PPA* rises and *PA* falls again, *BPPA2* is pulled down and MN1 is turned off. Then, *PD* is

Fig. 2. Proposed bootstrapped ring oscillator: (a) unit delay cell structure, (b) N-stage implementation

boosted below ground by a capacitive coupling by C_{PD} , resulting in an increased driving strength of MN2 to speed up the pull down transition of the output.

As in the conventional ring oscillator, the proposed ring oscillator provides an increased oscillation frequency based on voltage bootstrapping. On top of that, since the boosting operation is initiated not by the signal from the first previous stage but by an earlier signal coming from the third previous stage, timing criticality through the boosted signal paths can be relieved, resulting in higher speed gain. Hence, by adapting the proposed ring oscillator, a higher oscillation speed can be obtained for the same supply voltage, or an identical speed performance can be achieved at lower supply voltage, resulting in power reduction. The reduced timing mismatch between the signals to the gate and source of driver transistors, which was the problem in the conventional circuit in Fig. 1, also allows further speed gain and power reduction. The fact that the on/off control of precharge transistors is done not by the current stage output but by a feedforward input also prevents boosted charge loss and plays a role on speed improvement and power reduction.

4 Comparison and discussion

The proposed ring oscillator and conventional ring oscillator [10] are designed in a 65 nm CMOS technology, whose simulation results are summarized in Fig. 3. The supply voltage range for the simulation is from 0.35 V to 0.6 V, and the boosting capacitor size is 50 fF. Fig. 3(a) and (b) depict the simulated waveforms of the conventional and proposed oscillators at 0.5 V, respectively. The voltage waveforms indicate that the proposed ring oscillator has lower latency per stage and thus higher oscillation frequency. The current waveforms per stages also indicate that, although the peak current of the proposed delay cell is larger than that of the conventional delay cell due to fast transitions, total amount of charge consumed during one period is substantially reduced, resulting in lower power consumption. The latency and power consumption of the conventional and proposed unit delay cells depending on supply voltage are compared in Fig. 3(c). The proposed unit delay cell has lower latency with smaller power consumption majorly due to signal feedforwarding. The latency is reduced by 30.8%~50.8% with up to 23.5% power reduction. The maximum oscillation frequency and average power consumption in terms of supply voltage for the conventional and proposed 7-stage ring oscillators are shown

Fig. 3. Performance comparison: (a) simulated waveforms (conventional), (b) simulated waveforms (proposed), (c) latency/power versus supply voltage (unit delay cell), (d) oscillation frequency/power versus supply voltage (7-stage ring oscillator), (e) ring oscillator oscillation frequency versus stage number

in Fig. 3(d). With the proposed ring oscillator, the oscillation frequency is increased by 44.5%~103.3%, and the power consumption is reduced by 17.6%~23.5%. We designed a set of ring oscillators having several different numbers of stages, whose performance comparison results are depicted in Fig. 3(e). For the conventional, 5-stage ring oscillator is the minimum stage implementation. For the proposed, 7-

stage ring oscillator turns out to be the minimum stage implementation since feedforward inputs from multiple previous stages reduces the effective number of stages visited by the signal traveling through the loop. Note that the conventional ring oscillator even with the minimum number of stages (1.69 GHz) can never reach the oscillation frequency obtained by the proposed ring oscillator (2.60 GHz). Note also that the oscillation frequency of the conventional 5-stage ring oscillator at 0.60 V (dotted circle on the left) is comparable to that of the proposed 7-stage ring oscillator operating at 0.50 V (dotted circle on the right). In this case, the energy consumption is 81.8 fJ for the conventional and 63.3 fJ for the proposed, implying 22.6% reduction. These results indicate that the proposed ring oscillator has far higher oscillation frequency, and consumes much less energy for providing the same oscillation frequency.

5 Conclusion

A novel bootstrapped ring oscillator is proposed in this paper. It has multiple feedforward connections for enhancing the speed and energy efficiency at ultra-low voltage region. The evaluation results in a 65 nm technology indicate that the proposed ring oscillator has improvements in terms of maximum achievable oscillation frequency and energy consumption for providing the same oscillation frequency.

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