An ultra-low-voltage self-powered energy harvesting rectifier with digital switch control

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Abstract: This paper presents an ultra-low-voltage high-efficiency interface circuit for energy harvesting, which features self-powered design and digital switch control. The proposed rectifier includes bridge rectifier and active diode. The former introduces self-driven switches and ultra-low voltage divider to reduce the voltage drop for wide output voltage swing. The latter adopts a common-gate comparator as switch control block to output a nearly digital signal, thereby improving dynamic response and anti-noise ability. The entire circuit exhibits good conversion efficiency and stability. Its minimum input voltage is down to 225 mV. The maximum voltage efficiency reaches to 96.3\%, supplying the output current of 29 µA and the output power of 15.43 µW. The maximum power efficiency is 96.5\%, providing the output current of over 16.1 µA and the output power of 5.19 µW. The whole circuit consumes the power loss of 1.42 µW.

Keywords: energy harvesting, rectifier, ultra-low-voltage, self-powered, digital switch control

Classification: Integrated circuits

References

1 Introduction

Widespread concerns on environmental pollution and energy consumption are driving the development of energy harvesting, which scavenges energy from the ambient sources to power the long-lived, maintenance-free systems, as the replacement or recharge of batteries. Usually the received energy is diminutive AC power, so a high-efficiency rectifier has become the key for energy harvesting systems. The primary design challenges are to maximize energy transfer and minimize power loss. This paper presents a feasible rectifier with digital switch control under ultra-low-voltage, which is characterized by high conversion efficiency and low power loss. The proposed rectifier adopts self-driven switches with ultra-low-voltage divider to increase the output voltage and uses common-gate comparator outputting a nearly digital signal to improve dynamic response and system stability. The circuit is fabricated in 65-nm CMOS process. The paper is organized as follows. The proposed rectifier is detailed in Section 2; the simulation results are presented in Section 3; a conclusion is followed in Section 4.

2 Design of the proposed rectifier

The proposed rectifier adopts two stage structures, as shown in Fig. 1. The first stage is bridge rectifier that converts AC to DC outputting a positive half-wave voltage. The second stage is active diode that uses digital switch signal to control charging or discharging of the storage capacitance, and its output voltage supplies the entire circuit. To maximize energy transfer, the rectifier should be able to operate under ultra-low-voltage with high efficiency and fast dynamic response speed [1].

2.1 Bridge rectifier

The proposed rectifier is composed of self-driven switches and ultra-low voltage divider, as revealed in Fig. 2. The self-driven switches are directly driven by AC input voltage, which maximizes the gate-source voltage, thereby improving the loading capability and the minimum energy available. The substrate potential of NMOS is connected to the drain, to introduce the bulk-source voltage drop, which reduces the threshold voltage effectively, as derived in Eq. (1).

\[
V_{th} = V_{th0} + \gamma (\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})
\]  

(1)

Obviously, a weak positive bias bulk-source voltage \(V_{BS}\) could reduce \(V_{th}\), and then reduce the required power supply. As a result, the power loss is greatly saved. In addition, small \(V_{th}\) results in small on-resistance \(R_{on}\). Under low input voltage,
these four switches work in linear region alternately. Because the output voltage of bridge rectifier is in proportion to $1/R_{on}$, so $V_{BS}$ improves the output voltage. But $V_{BS}$ inevitably introduces poor noise suppression ability and frequency characteristic. Nonetheless, the self-driven switches still perform well in small input voltage range, as long as the antenna matching network is good enough. Large device could also reduce $R_{on}$, but at the cost of die size and parasitic effects. It is worth noting that $V_{BS}$ must be smaller than 0.3 V, otherwise, the parasitic transistor will conduct to cause large leakage current. Considering the process compatibility, the drain and bulk of NMOS are simply connected to ground. The drain of PMOS is connected to the output $V_A$, and the bulk is biased by an ultra-low voltage divider. The voltage divider provides lower bulk potential than the drain potential, which increases the output voltage swing. Compared with NMOS dividers in Refs. [2] and [3], this divider has lower output resistance and faster dynamic response, and it is more suitable for ultra-low-voltage working. Its supply voltage is provided by the output of active diode, which is self-powered.

![Fig. 2. The proposed bridge rectifier circuit](image1)

### 2.2 Active diode

As displayed in Fig. 3, a large PMOS MPS is adopted as active diode for small conduction loss but large parasitic capacitor, which puts forward challenges to system stability. The design key lies in the control circuit and bulk regulation. The former improves the switching speed and reduce conduction loss. The latter eliminates parasitic effects, especially leakage current. A novel common-gate comparator is used as control block to switch the active diode, as detailed in Fig. 4. It outputs a clean digital pulse signal and nearly does not consume power. The performance of active diode greatly depends on the comparator. MPB1 and MPB2 and MPB3 are used as bulk regulation circuit to bias the bulk of MPS. The power supply is extracted from the output $V_C$, which removes external power supply to save die size and power loss.

![Fig. 3. The active diode with control circuit](image2)
The proposed comparator is consists of three parts. The start-up block assures the circuit to work from zero-state. Once the comparator begins to work, the start-up block shuts off to save power. The input block is composed of differential input common-gate transistors (MN7/MN8) and current mirror loads (MP6/MP7). It provides high gain with low input-resistance and high output-resistance. The voltage redundancy consumed by the input stage is equal to $2V_{ov} + V_{th}$, where $V_{ov}$ is saturation voltage drop. Compared with the bulk-driven input stages in Refs. [2] and [3], this work has better noise suppression capability, with almost the same voltage redundancy. Furthermore, because there is no miller capacitor product in input stage, the comparator achieves wider bandwidth and less parasitic effects. The output stage uses noninverting schmitt trigger to speed up switching and remove noise, depending on positive feedback hysteretic loop. Only voltage gain is supplied to drive MPS, which helps to reduce parasitic effects. This comparator generates a nearly digital signal to control MPS and bulk regulation circuit, and provides fast dynamic response and strong anti-noise ability, with little power loss.

As revealed in Fig. 4, when $V_{in-} (V_A)$ is larger than $V_{in+} (V_C)$, MN8 turns on and extracts current from the drain, MPS opens. The harvested energy is stored in $C_L$ and supplies loads. Conversely, MPS is close, and $C_L$ provides power supply for loads. The digital control is a promising solution for low-power high-efficiency design. The bulk regulation circuit connects the bulk of MPS to higher potential for small conduction loss and large output current. When MPS turns on, its bulk is connected to $V_A$ by MPB1. Now the bulk-source voltage $V_{BSS}$ of MPS equals to the source-drain voltage $V_{DSB1}$ of MPB1. MPB1 prevents pn-junctions open during start-up and avoids latch-up [4, 5]. The width of MPB1 should be small enough to reduce $V_{DSB1}$, thereby against its own pn-junction conduction leakage current and power loss. MPB2 makes the same work when MPS shuts off. Compared with the bulk regulation circuit in Ref. [5], the bulk of MPB1/MPB2 is also attached to high potential, which helps to reduce the voltage drop. To safely open MPS in all process corners, a bypass diode MPB3 is added in parallel with MPS [2, 3].

3 Simulation results

The entire circuit is detailed in Fig. 5. Where $R_{in}$ is internal resistor of $V_{in}$, $C_{in}$ is internal capacitor, $V_{drop}$ is voltage drop across transistors. $V_A$ is decided by Eq. (2).
\[ V_A = V_{in} - i_m R_{in} - 2 V_{drop} = V_{cin} - 2 V_{drop} \]  

(2)

\( R_{in} \) introduces a little of power loss. At the same time, \( C_{in} \) leads to the lag during energy transfer. \( C_{in} \) is charged during the positive half cycle of \( V_{in} \). When \( V_{in} \) becomes negative, \( C_{in} \) is discharged first before it is charged to negative, and vice versa. It delays the switching of bridge rectifier and wastes energy. Although the input source is not ideal, the antenna matching network could weaken its impact on the system performance slightly.

The rectifier is simulated in 65-nm CMOS process. Supposed \( V_{in} \) is 500 mV with 100 Hz, \( R_{in} \) is 50 mΩ, \( C_{in} \) is 25 nF, \( R_L \) is 20 kΩ, \( C_L \) is 10 µF, which balance the tradeoff between conversion efficiency and power. Fig. 6(a) shows the voltage efficiency \( \eta_V \) as a function of \( V_{in} \) at different process corners, as calculated in Eq. (3).

\[ \eta_V = \frac{V_{out}}{V_{in}} \times 100\% \]  

(3)

Under typical conditions, the output voltage increases slightly once \( V_{in} \) is beyond 225 mV. At 275 mV the output voltage begins to increase rapidly because active diode starts working. Once \( V_{in} \) is larger than 450 mV, \( \eta_V \) is over 90%. When \( V_{in} \) is 550 mV the system reaches to optimum working point with maximum \( \eta_V \) of 96.3%, providing the output current \( I_{out} \) of 29 µA and the output power \( P_{out} \) of 15.43 µW. Afterwards, \( \eta_V \) keeps higher than 93.7%, which benefits from low \( V_{drop} \) of switches. Self-driven bridge rectifier with ultra-low voltage divider makes \( V_{drop} \) as small as possible, which greatly improves \( V_A \). At the same time, both the comparator and bulk regulation block reduce the on-resistance and leakage current of MPS, thereby enhancing \( V_C \) and loading capacity. The comparator only extracts
a little energy from $C_L$ and saves power. Compared with the rectifier in Ref. [3], the system performance is improved significantly.

The voltage efficiency is further investigated at different loads, as shown in Fig. 6(b). Visibly, the rectifier has a wide loads matching range. With the increase of $R_L$, $\eta_V$ rises up slightly, and the minimum working voltage declines. This is because that the decreasing load current leads to the smaller conduction voltage drop on MPS and enhances the discharge cycle. The simulation results indicated the rectifier has a good load regulation.

The power efficiency $\eta_p$ is plotted in Fig. 7(a) against $V_{in}$ at different process corners, as defined in Eq. (4).

$$
\eta_p = \frac{P_{out}}{P_m} \times 100\% = \frac{1}{T} \int_{t}^{t+T} \frac{v_{ou}t_i_{ou}}{t_{in}i_{in}dt} \times 100\% \tag{4}
$$

The maximum $\eta_p$ is 96.5% at $V_{in}$ of 500 mV under typical conditions. At this time the rectifier provides $I_{out}$ over of 16.1 $\mu$A and $P_{out}$ of 5.19 $\mu$W. After then, $\eta_p$ decreases gradually. It is due to that with the increase of $V_{in}$, the current consumed by transistors increases, which results in much power loss. Especially, when the power loss increases close to $P_{out}$, $\eta_p$ maybe reduces to 50%. Nevertheless, $P_{out}$ provided is still increasing. The maximum $\eta_p$ appears a little earlier than the maximum $\eta_V$ with the increasing $V_{in}$.

In order to verify the feasibility of the proposed rectifier, Table I. lists the performance comparison of the up-to-date interface circuits for energy harvesting. It is difficult to make a fair comparison between different interface circuits because that the system performance is limited by many factors, such as ambient energy.
sources, antenna matching circuits, process conditions, etc. The proposed rectifier performs relatively well. It starts to work at $V_{\text{in}}$ of 225 mV and provides almost the same level output voltage. The rectifier in Ref. [2] has good conversion efficiency and low input voltage. But its stability and simplicity are slightly worse. The rectifier in Ref. [3] has lower input voltage of 150 mV, but its conversion efficiency is slight low. The rectifier in Ref. [7] has large enough output power but at the cost of poor output current and conversion efficiency. The rectifier in Ref. [8] has good performance but is not suitable for ultra-low-voltage application. The rectifier in Ref. [6] has large die size and power loss in exchange for good performance. The rectifier in Ref. [4] performs very well except the rectified voltage range. Comparatively speaking, the proposed rectifier offers good conversion efficiency and the competitive output current and output power. Moreover, the entire system power loss is only 1.42 µW. The low power loss primarily benefits from self-driven transistors with ultra-low-voltage divider and common-gate comparator that provides digital control. Consequently, the proposed rectifier exhibits a few advantages and is worth being researched further.

### 4 Conclusion

The proposed ultra-low-voltage self-powered energy harvesting rectifier uses the self-driven switches with ultra-low-voltage divider and digital switch design to greatly improve the performance of system. Its input voltage is down to about 225 mV, and the entire power loss is only 1.42 µW. The rectifier is able to drive wide output load range with the voltage efficiency of over 93.7%, as well as the maximum power efficiency of 96.5%. It provides an output current of 29 µA and output power of 15.43 µW, which will increase with the input voltage. The proposed rectifier displays good overall performance, and is suitable to the ultra-low-voltage ultra-low-power applications.

### Acknowledgments

This work was supported by the Young Scientists Fund of the National Natural Science Foundation of China (Grant No. 61306044), the National Science Fund for Excellent Young Scholars of China (Grant No. 61322405), the National High Technology Research and Development Program of China (Grants No. 2012AA012302 and 2013AA014103).