A 0.017 μ J/sample 313 K sample/sec clamped sensing-based time domain CMOS temperature sensor

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Abstract: This paper describes the design of a CMOS temperature sensor intended to compensate for the thermal effect of NAND Flash cells. The temperature sensor is mainly composed of a SENSOR part and COUNTER part. The SENSOR part generates a pulse (T_{PTAT}); its width is proportional to absolute temperature (PTAT). Furthermore, the clamped sensing scheme is used to eliminate the effects of temperature and process skew variation of sensing circuits. The COUNTER part converts T_{PTAT} to digital codes. The proposed temperature sensor consumes a 0.017 μ J/sample at a conversion rate of 313 K sample/sec.

Keywords: CMOS temperature sensor, clamped sensing, PTAT, temperature coefficient

Classification: Integrated circuits

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1 Introduction

Temperature sensors manufactured in the CMOS process are attractive because they greatly reduce the cost and can be used directly on on-chip interface with other circuits to compensate for thermal effects. For example, in NAND flash memory, as shown in Fig. 1(a), there are multiple states (“A”, “B” and “C”) of the cells’ V_{TH} distributions to store multiple data in memory cells. Fig. 1(b) shows that read margins of the NAND Flash memory cells are reduced because the NAND flash memory cells are highly sensitive to temperature variations. Therefore, a specific type of V_{READ} generator [1] is needed to compensate for the thermal coefficient of cells V_{TH} variations as seen in Fig. 1(c). However, to compensate for different kinds of thermal effect (e.g., temperature effect of erase efficiency [2]), there is in need for other compensation circuits. The most effective way to prevent duplication is using the temperature sensor to compensate for various thermal effects.

Fig. 1. Temperature V_{TH} shift of NAND Flash memory cells: (a) V_{TH} distribution at room temperature; (b) narrow read margin due to V_{TH} temperature variations; (c) compensation of V_{TH} temperature variations with temperature.

In particular, a high conversion rate is essential for prevention of performance (read, program, and erase throughput) degradation of NAND Flash memory. Usually, in NAND Flash memory, a conversion rate of more than 200 K sample/

sec does not actually affect the NAND Flash performance as it takes more than 5 μ s to initialize the micro controller of NAND Flash memory.

There are many temperature-sensing schemes reported in the literature [3, 4, 5, 6, 7, 8, 9, 10, 11, 12]. Bandgap temperature sensors based on analog-to-digital converter (ADC) [3, 4, 5, 6] show a relatively high level of accuracy, but they occupy a large area and have high power consumption levels. Time domain temperature-dependent delay line-based temperature sensors [7, 8, 9, 10] are reported. However, inverter delay varies not only temperature but also process skew. Therefore, each sensor needs calibration according to its process variation. A time domain temperature sensor with dual delay-locked loops (DLLs) scheme has been reported [11], but it required additional DLLs area as well as crystal oscillators to operate DLLs. A time domain leakage-based temperature sensor is addressed [12], but conversion rate is inverse proportional to exponential of temperature, so performance is seriously degraded at low temperatures.

In this work, we designed a time domain temperature sensor for compensating for the temperature coefficient of NAND Flash memory cells. Digital codes of the temperature sensor are generated by counting the measurement time, which is discharge time of capacitor, similarly to [12]. The main differences of this work are improvement in conversion rate and elimination of temperature and process variation of sensing circuits.

2 Operating principle

Fig. 2 shows the concepts of the proposed temperature sensor. This temperature sensor is mainly composed of a SENSOR part and a COUNTER part. The SENSOR part is composed of T_{REF} GEN and T^*_{PTAT} GEN blocks, and it generates a pulse with width proportional to absolute temperature (PTAT) (T_{PTAT}). The T_{PTAT} is generated by exclusive OR arithmetic operation of T_{REF} and T^*_{PTAT} . T_{REF} and T^*_{PTAT} are generated by T_{REF} GEN and T^*_{PTAT} GEN, respectively.

Fig. 2. Block diagram of the proposed temperature sensor.

Fig. 3 shows the principles of the proposed sensing scheme. In case of capacitor (C) discharged to a voltage variation (ΔV) through a constant current source (I), the capacitor discharge time (ΔT) is estimated as:

$$\Delta T = \frac{\Delta V \cdot C}{I} \quad (1)$$

The same principle holds to eq. (3) and eq. (5).

Fig. 3. Capacitor discharge through the constant current

The circuit and timing diagram of the T_{REF} GEN shown in Fig. 2 are in Fig. 4(a) and (b). In the T_{PRECH} phase, transistor M1 is turned on, and VC is clamped pre-charge to $V_{PRE}-V_{THN.M2}$ through sense out (SO) node and transistor M2. After T_{PRECH} phase, the VSENSE node is biased to a voltage of V_{SEN} ($V_{SEN} < V_{PRE}$). During the $T_{EVALUATION}$ phase, VC is discharged through a zero temperature coefficient current source (I_{ZTC}). In case of $V_{VC} > (V_{SEN}-V_{THN.M2})$, M2 is turned off; therefore, SO maintains the voltage at the VDD. If $V_{VC} < (V_{SEN}-V_{THN.M2})$ M2 is turned on, then charge sharing occurs between SO and VC. The capacitance C in the VC is larger than the SO; therefore, the voltage level of SO is followed by the VC. Due to clamped pre-charge and sensing through the same transistor, M2, the temperature and process variation of $V_{THN.M2}$ are canceled out, so the voltage ΔV_{VC} in Fig. 4(b) is equal to $V_{PRE}-V_{SEN}$. For improved conversion rate, ΔV is must be a small value. Transistor M2 in Fig. 4(a) acts as an amplifier, and the DC gain of M2 can be estimated as:

$$A_{V.M2} = \frac{\Delta V_{SO}}{\Delta V_{VC}} = \frac{(VDD - V_{SEN} + V_{THN.M2})}{\Delta V_{VC}} \quad (2)$$

Therefore, the inverter which is composed of M4 and M5 is under the stable operating condition with large input range. The static characteristics of the clamped sensing scheme as described in Fig. 5.

Fig. 4. T_{REF} GEN: (a) schematic of T_{REF} GEN block; (b) timing diagram of T_{REF} GEN block.

Fig. 5. The static characteristics of the clamped sensing scheme.

T_{REF} is expressed by the following equation, similar to equation (1):

$$T_{REF} = \frac{\Delta V_{VC} \cdot C}{I_{ZTC}} = \frac{(V_{PRE} - V_{SEN}) \cdot C}{I_{ZTC}} \quad (3)$$

The circuit and timing diagram of the T^*_{PTAT} GEN shown in Fig. 2, are shown in Fig. 6(a) and (b). After clamped pre-charge of the VC_{PTAT} to $V_{PRE} - V_{THN.M2}$, additional pre-charge current, I_{PTAT} , is integrated to C in VC_{PTAT} during the T_{PTAT_PRECH} . After the additional pre-charge of the VC_{PTAT} , its voltage level is expressed by the following equation.

$$VC_{PTAT.ADD} = V_{PRE} - V_{THN.M2} + \frac{I_{PTAT} \cdot T_{PTAT_PRECH}}{C} \quad (4)$$

Therefore, T^*_{PTAT} can be expressed as:

$$T^*_{PTAT} = \frac{C \cdot \Delta V^*_{VC_{PTAT}}}{I_{ZTC}} = \frac{C \cdot (V_{PRE} - V_{SEN}) + I_{PTAT} \cdot T_{PTAT_PRECH}}{I_{ZTC}} \quad (5)$$

As mentioned in Fig. 2, the T_{PTAT} is generated by exclusive OR arithmetic operation of T_{REF} and T^*_{PTAT} ; therefore, T_{PTAT} can be estimated as:

$$T_{PTAT} = \frac{Q_{PTAT}}{I_{ZTC}} = \frac{I_{PTAT} \cdot T_{PTAT_PRECH}}{I_{ZTC}} \quad (6)$$

In eq. (6), T_{PTAT} seems to be irrelevant to C , but when VC_{PTAT} is pre-charged during T_{PTAT_PRECH} , small C causes inaccuracy of sensing due to large $\Delta V_{VC_{PTAT}}$, and channel length modulation is worsened by large ΔV , so there are differences in I_{ZTC} between T_{REF} GEN and T^*_{PTAT} GEN blocks.

Fig. 6. T^*_{PTAT} GEN: (a) schematic of T^*_{PTAT} GEN block; (b) timing diagram of T^*_{PTAT} GEN block.

Fig. 7 shows the timing budgets of the proposed temperature sensor, and design parameters are summarized in Table I. The proposed temperature sensor needs a stable clock for the counter to convert from T_{PTAT} to digital code. As a clock for the counter, a micro clock of an on-chip NAND Flash memory or data clock from a NAND Flash controller are available. In this design, the counter is operated by data clock of 200 MHz. It takes about 3.2 μ s to convert temperature to digital code. Therefore, conversion rate performance of the proposed temperature is 313 k samples/sec.

Table I. Design parameters of proposed sensor

Parameter	Description	Value
C	Capacitor in T_{REF} GEN and T_{PTAT}^* GEN.	2 pF
I_{ZTC}	Zero temperature coefficients current	1 μ A
ΔI_{PTAT}	The difference of I_{PTAT} between -40°C and 120°C	20 μ A
V_{PRE}	The bias voltage of V_{SENSE} during T_{PRECH}	1.5 V
V_{SEN}	The bias voltage of V_{SENSE} during T_{PTAT}^*	1.4 V
f_{CLK}	Clock for counter	200 MHz

Fig. 7. The timing budgets of the proposed temperature sensor.

3 Circuit details

A PTAT bias current [13] (I_{PTAT}) is chosen to pre-charge the $V_{C_{PTAT}}$ during the T_{PTAT_PRECH} . It is clear that, in order to generate T_{PTAT} , a biasing current with a positive temperature coefficient is required. In particular, when high resolution of temperature sensing is needed, it takes a long time for digital output of T_{PTAT} by counting blocks. Therefore, to pre-charge more Q_{PTAT} in a T_{PTAT_PRECH} , slope control of I_{PTAT} is required. The I_{ZTC} generation circuit is shown in Fig. 8(a). The I_{ZTC} mirrored current of the I_{REF} by the aspect ratio of the M2 and M3. The I_{ZTC} can be estimated as:

$$I_{ZTC} = I_{REF} \cdot \frac{(W/L)_{M3}}{(W/L)_{M2}} \quad (7)$$

I_{REF} is expressed by the following equation.

$$I_{REF} = \frac{V_{BGR}}{R} \quad (8)$$

To mitigate the temperature coefficient of I_{REF} , the R is composed of positive and negative temperature coefficient resistors. The I_{PTAT} generation circuit description is shown in Fig. 8(b). The $A \cdot I_{PTAT_BG}$ is a mirrored current of the I_{PTAT_BG} by A times. To remove the offset of $A \cdot I_{PTAT_BG}$, $B \cdot I_{ZTC}$ is needed. The $B \cdot I_{ZTC}$, is a mirrored current of the I_{ZTC} by B times. In Fig. 8(b), I_{PTAT} is can be estimated as:

$$I_{PTAT} = A \cdot I_{PTAT_BG} - B \cdot I_{ZTC} \quad (9)$$

In eq. (9), the I_{PTAT_BG} is copied from a bandgap reference circuit [14]. Fig. 9(a) illustrates the generation process of I_{PTAT} . Fig. 9(b) shows the simulation results of I_{ZTC} and I_{PTAT} under a temperature range of -40°C – 120°C .

Fig. 8. A PTAT biasing circuit: (a) I_{ZTC} generator; (b) I_{PTAT} generator

Fig. 9. (a) Generation process of I_{PTAT} ; (b) simulation results of I_{ZTC} and I_{PTAT} .

4 Measurement results

The proposed temperature sensor is fabricated in a 0.35- μm CMOS process, as shown in Fig. 10 and its active area is 0.2 mm². The measured results of the proposed temperature sensor's output codes and errors after two-point calibration are shown in Fig. 11(a) and (b), respectively. The resolution of the temperature sensor is 0.44°C/LSB, and inaccuracy is -1.5°C – 2.2°C over a temperature range of -40°C – 100°C . Table II summarizes the performance of the proposed temperature sensor and compares it with previous time domain temperature sensor designs.

Fig. 10. Die microphotograph.

Fig. 11. Measurement results after two-point calibration: (a) Measured digital output code; (b) Measured errors

Table II. Comparison of time domain temperature sensors

	Range (°C)	Error (°C)	Energy (μJ/sample)	Conversion Rate	Resolution (°C)	Area (mm ²)	CMOS process (μm)
This work	-40–100	-1.5–2.2	0.017	313 k	0.44	0.2	0.35
[7]	0–100	-0.7–0.9	5	2	0.16	0.175	0.35
[8]	-40–95	-0.8–0.8	0.45	20	0.523	0.4	0.35
[9]	0–75	-1.5–0.8	4.2	5	0.058	N/A (FPGA)	FPGA
[10]	-40–60	-0.6–0.6	0.3	2	0.09	0.09	0.35
[11]	0–100	-4.0–4.0	0.24	5 k	0.78	0.12	0.13
[12]	20–100	-1.97–1.97	0.0011	12	0.28	0.01	0.35

5 Conclusions

In this work, we developed a clamped sensing-based time domain temperature sensor in a 0.35 μm CMOS process. The proposed sensor occupies 0.2 mm² in 0.35 μm CMOS process and consumes 0.017 μJ/sample at a conversion rate of 313 k sample/sec. The resolution of the temperature sensor is 0.44°C/LSB and inaccuracy is -1.5°C–2.2°C over a temperature range of -40°C–100°C. This proposed temperature sensor with low power consumption and high conversion rate is well suited for temperature compensation of NAND Flash memory cells.

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