A 270-MS/s 6-b SAR ADC with preamplifier sharing and self-locking comparators

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Abstract: This paper presents a high speed SAR ADC with distributed comparators and shared preamplifiers. In contrast with the previous design, the sharing preamplifier technique avoids input range degradation and comparators' offset calibration. Also, the paper proposes a self-locking dynamic comparator to maintain its high speed and high robustness. Moreover, it consumes less power than traditional single cross-coupling comparator. The ADC is fabricated in 0.13 μm CMOS technology to achieve a performance of 6-b resolution at 270-MSps rate. Its power consumption is 4.25 mW under a supply of 1.2 V. The measurement results shows the ADC achieves an ENOB of 5.65b with a low frequency input and 5.17b with a up-to-Nyquist frequency input. The FoM of the proposed ADC is 313-fJ/conversion step.

Keywords: successive approximation register, analog-to-digital converters, preamplifier, comparators

Classification: Integrated circuits

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1 Introduction

Modern communication systems need up-to-hundred-mega-hertz low resolution and low power ADCs as key parts such as ultra-wide band (UWB) communication systems, hand-held imaging devices and portable instruments. Traditionally, these ADCs are implemented by flash/folding ADCs [1, 2], where only forward paths are involved in the ADC's mechanism. These forward-path-only structure can be

further accelerated by pipelined structure. However, as the CMOS technology progress, the flash topology is well known for its power hungry character. The figure of merit (FoM) value is very likely to exceed 1 pJ/conv.step, because the number of comparators increases exponentially with one more bit.

Asynchronous SAR (successive approximation registered) ADCs were chosen as hundred-MHz ADC firstly in [3]. Compared with flash and folding counterparts, only one comparator is needed in a conventional SAR ADC. Every time the decision bit is made, it feeds back a control signal to the front end capacitive tank. The drawback of SAR ADCs is that more time would spent on the feedback settling path. Fortunately, thanks to the advanced process, it is not difficult for SAR ADC to achieve such fast speed. However, those previous designs on high speed, low power and resolution ADCs requires complex calibration. In [3], a non-binary (radix 1.81) capacitor array was proposed to generate redundancy, thus tolerating incomplete settling. However, this radix cannot be implemented precisely by manually choosing capacitors with special sizes. Process, voltage and temperature (PVT) variation requires a complex digital calibration machine to detect and compensate the mismatch.

This paper presents a high speed asynchronous 6-bit SAR ADC which avoids comparators' offset calibration. The ADC topology distributes and self-locks all the comparators to save the DFF delay in the critical paths. An extra and shared preamplifier is proposed to overcome drawbacks introduced by distributing comparators.

2 SAR ADCs eliminating D-FF induced delays

Modern SAR ADCs' speed is limited by the loop delay from one comparison to the next [4]. Eq. (1) shows the critical path of the loop delay, as the circuits imply in Fig. 1(a):

$$T_{critical} = T_{comp} + T_{digital} + T_{\tau}, \quad (1)$$

where T_{τ} is an approximation on the DAC settling time. Among these timing parts, the longest useless one is the DFF delay in the digital logic delays, $T_{digital}$.

In [4], the first SAR ADC with distributed comparators was proposed, as shown in Fig. 1(b). By distributing one comparator for every comparison, the D-FF induced delay are eliminated. Thus, the critical paths delay is evolved to

Fig. 1. Critical path in (a) conventional SAR ADCs (b) SAR ADCs distributing comparators in [4].

$$T'_{critical} = T_{comp} + T_{XOR} + T_{\tau}. \quad (2)$$

The method accelerates SAR ADCs to an extent of 1.5x-2x in every comparison.

However, this method directly connects the top plate of the capacitive DAC to all the comparators. Given the high speed of these comparators, big kickbacks may ruin the conversion resolution. In [4], a 17x unit capacitor was inserted in the capacitive DAC to absorb the kickbacks, which degrades the input range and LSB amplitude largely. As a result, the comparator needs a tighter constraints on the offset issues and a 7-b binary DAC was applied to all the comparators to cancel these offset issues.

3 Proposed SAR ADC architecture

As an high speed design, the proposed ADC still utilizes the distributed comparator topology to eliminate the D-FF induced delay. However, a shared preamplifier is used to prevent the design from input range degradation and comparators' calibration, as shown in Fig. 2.

The signals are first sampled on all the capacitors. After that, a pre-amplifier bridges the capacitive DAC and the distributed comparators. Each comparison generates one bit decision and holds the result until the conversion ends. Only simple logics (mainly driving inverters) is on the critical feedback path in the design. The SAR employs an asynchronous fashion, which means every comparison starts when an enable signal generated by last comparison reaches. Note that T'_{τ} should include an approximation of the preamplifier delay.

$$T'_{\tau} = T_{CapDAC} + T_{SharedPA}. \quad (3)$$

There are three main advantages on the proposed pre-amplifier sharing. First, the preamplifier isolated the capacitive DAC and the comparators, and thus, kickback will not influence the charge conservation nodes. Furthermore, given that no capacitors are inserted to absorb the kickbacks and the charge conservation nodes are with less parasitic (only one-preamplifier input instead of six-comparator input), the input range and the LSB amplitude is much larger than that of [4]. The last advantage is the conventional preamplifier's benefits, fixing latches' input common mode voltages and amplifying signals fed to comparators. These benefits relax the comparator design and enhance its speed. All these advantages produce a high-speed and calibration-free implementation of the 200-MSps 6-b SAR ADC in 0.13 μm CMOS technology.

Fig. 2. Proposed SAR ADC's architecture

4 Circuit implementation

4.1 Self-locking dynamic comparator

In the design, all the six comparators are distributed. After comparison, its decision should be held until the conversion ends. However, during this hold time, the input of the comparators varies due to those decided bits' feeding back to the DAC. Chances are that a huge input change causes metastability, or even a wrong result in those already decided bit. Authors would like to call this effects as *flashback* effects. In [4], a strongARM comparator, or known as a dual cross-coupling comparator was used to reduce the possibility of these flashback effects.

In fact, the dual cross-coupling comparators cannot eliminate the flashback completely. Also, compared with those single cross-coupling comparators, the dual one suffers from lower speed, though it is more robust [5].

The design proposed a self-locking technique to completely remove the flashback issue and use single cross-coupling comparators to achieve high speed. Fig. 3(a) shows the topology of the self-locking comparator.

Fig. 3(b) also demonstrates the timing diagram of the self-locking comparator. Before the comparator was enable, the two outputs are pulled down by M5 and M6. M2 is off as well. When the EN_i arrives, the single cross-coupled regenerative latch is released. After the positive feedback push the differential outputs to be 1 and 0 respectively, a XOR gate turns the M2 off. In other words, it automatically locks the comparator. Since there is no power to drive the two input transistors, M3 and M4, the outputs will be fixed after self-locking. By this way, the flashback effects will not take place even when the inputs vary. Another positive side effect of the self-locking comparator is its low power character. For traditional single cross-coupling comparators, its high logic voltage is likely to much less than VDD. It implies a quasi-static power consumption during comparator holding its decision. However, the self-locking process removes this quasi-static power consumption by turning M2 off. This power saving is especially effective for the long holding comparators like the first one.

Note that by the time the i -th comparator is locked, the enable signal of the $(i + 1)$ -th comparator, EN_{i+1} , has been generated too. Also, after the last comparator distinguishes its decision, All the comparators and switches are reset to the

Fig. 3. (a) Self-locking comparators. (b) Timing diagram of the self lock process.

initial case. Considering that all these gates are on critical paths, high speed logic topology are chosen here. The XOR gates and OR gates are implemented by transmission gate logic and dynamic logic with voltage reservation transistors.

4.2 Shared preamplifier

The shared preamplifier is made by a PMOS-input common source amplifying circuits with resistive load. Considering the PMOS input of the comparators, the resistive load can provide lower operating voltage at the output node than diode-connected NMOS load. By a small resistor, the preamplifier achieves a low gain but a wide bandwidth to track the capacitive DAC signal. Also, the input transistor is carefully designed to trade off kickback and speed. As the only device consumes static power in the ADC, the preamplifier dissipates 450 μ A under 1.2 V power supply.

4.3 Capacitive feedback DAC

The proposed ADC employs a 5-b binary capacitive DAC. It is an array composed by minimum MIM capacitors provided by the PDK. The switches procedure follows a monotonic fashion proposed in [5] to save the reference power consumption. By this way, a 2^5 x unit capacitor is saved, relaxing the sampling switch design. Also, the common mode voltage goes down after every comparison, increasing the gain of the preamplifier when the last few times comparison.

5 Measurement results

The proposed 270-MSps 6-b ADC has been fabricated in TSMC 0.13 μ m CMOS technology with 1.2 V power supply. The layout and the die micrograph is demonstrated in Fig. 4(a). At a clock rate of 270 Mhz, the ADC consumes 4.25 mW and achieves a peak SNDR of 35.394 dB and SFDR of 44.6 dB with frequency input. The output spectrum is demonstrated in Fig. 4(b). Fig. 5(a) shows the sampling frequency versus SNDR and SFDR at 200 MHz and 270 MHz clock rate respectively. The non-linearity characteristic is shown in Fig. 5(b), where DNL is less than ± 0.8 LSB and INL is less than ± 0.6 LSB. The ADC achieves an ENOB of 5.58b and a FoM of 313 fJ/conversion-step at 270 MHz.

Fig. 4. (a) The die micrograph. (b) Measured FFT spectrum.

Fig. 5. (a) Sampling frequency versus SNDR and SFDR. (b) DNL and INL of the proposed ADC.

6 Conclusion

A high speed SAR ADC with distributed comparators and shared preamplifiers is proposed in this paper. The shared preamplifier avoids disadvantage of the previous SAR ADCs with the distributed comparators. Also a self-locking dynamic comparator is designed to maintain its high speed and high robustness. The ADC is fabricated in 0.13 μm CMOS and achieves an ENOB of 5.65b at a rate of 270 MSps.

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