Investigation of in-situ doping profile for N+/P/N+ bidirectional switching device using Si$_{1-x}$Ge$_x$/Si/Si$_{1-x}$Ge$_x$ structure

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Abstract: We present a novel junction device with bidirectional current flow for switching devices in a high density spin torque transfer magnetic random access memory (STT-MRAM). In this structure, an N+ type strained SiGe material is adopted as a conduction layer to generate higher electron mobility and a flatter doping profile. A SiGe/Si/SiGe heterojunction structure is also used to obtain a better $I_{on}/I_{off}$ ratio due to a steeper junction profile. It is confirmed by 3D simulation that this structure provides higher current drivability and $I_{on}/I_{off}$ ratio. After the simulation, a junction device with N+ Si$_{0.8}$Ge$_{0.2}$/P Si/N+ Si$_{0.8}$Ge$_{0.2}$ and an area of 4 x 4 um$^2$ is fabricated and evaluated for bidirectional current flow. From the results obtained, we propose that this bidirectional switching device with a heterojunction structure is a promising candidate for a high density STT-MRAM.

Keywords: switching device, UHV-CVD, SiGe, N+PN+, STT-MRAM

Classification: Electron devices, circuits, and systems

References

1 Introduction

The scaling of selective devices in memory cells is a topic of great interest in recent memory technology. In recent years, several device technologies, such as vertical channel transistors (VCTs) and two terminal selective devices, have been reported [1, 2, 3]. Essential characteristics of a selective device include simple structure and high performance. In an STT-MRAM, a bidirectional current flow and high current drivability of more than $10^6$ A/cm$^2$ should be achieved for device operation [4]. VCTs provide good performance, but their structural complexity is a technological barrier [1].

In this work, we present a novel selective device providing bidirectional high current flow for an STT-MRAM. Here, SiGe material is used as the main conduction layer and a SiGe/Si heterojunction structure is adopted for high current drivability and an improved $I_{on}/I_{off}$ ratio. First, we compared the I-V characteristics of this structure under several structural conditions, and determined the best condition using device simulation. Then, a junction device was fabricated with N+ Si$_{0.8}$Ge$_{0.2}$/P Si/N+ Si$_{0.8}$Ge$_{0.2}$, and the cell characteristics were evaluated.

2 Device structure and simulation

Fig. 1a shows the schematic of the energy band diagram of the proposed Si$_{0.8}$Ge$_{0.2}$/Si/Si$_{0.8}$Ge$_{0.2}$ structure. It is expected that a strained Si$_{0.8}$Ge$_{0.2}$ layer with low dislocation has higher mobility than Si, which provides better current drivability compared to a structure with N+ Si/P Si/N+ Si only [3, 5]. In addition, we expect that the heterojunction structure of Si$_{0.8}$Ge$_{0.2}$/Si will provide a flatter N+ doping profile in the SiGe layer and a steeper junction profile at the interface of Si$_{0.8}$Ge$_{0.2}$/Si because it has a higher phosphorus incorporation rate than Si/Si only [6]. Fig. 1b shows the STT-MRAM structure using a junction device with a bidirectional switching device.

Here, the feature size of 4 F$^2$ for the STT-MRAM can be realized through this selective device by in-situ doped epitaxial growth on a Si substrate for the SiGe, Si, and SiGe layers. Fig. 2 shows the simulation results for the I-V characteristics under the junction structures of N+ (Si$_{0.8}$Ge$_{0.2}$)/P (Si)/N+ (Si$_{0.8}$Ge$_{0.2}$). In this simulation, the N type of $1 \times 10^{20}$, the P type of $3 \times 10^{18}$, and the N type of $1 \times 10^{20}$ atoms/cm$^3$ are applied to the junction layers, which are based on our previous work on Si/Si/Si structure [3].

First, we confirmed the dependency of the I-V characteristics at different lengths (15, 18, and 20 nm) of the P type Si layer, which is located in the middle. As shown in Fig. 2a, the group with a length of 20 nm showed the best performance with a current density of 1 MA/cm$^2$ and an $I_{on}/I_{off}$ ratio of $\sim 10^4$, which is acceptable for an STT-MRAM [4]. Moreover, after adjusting the slope of the
doping profile in the Si$_{0.8}$Ge$_{0.2}$ and Si interface, it was found that a steeper slope gives better performance, as shown in Fig. 2b. The 13.2 degree slope had a 51% higher current density than the 19.4 degree slope. From these simulation results, it is confirmed that the junction device provides good performance as a selective device under the conditions of Si$_{0.8}$Ge$_{0.2}$ with N doping of $1 \times 10^{20}$/cm$^3$ and a 20 nm length Si with P doping of $3 \times 10^{18}$ atoms/cm$^3$.

The flat doping and steep junction profile at the interface of Si$_{0.8}$Ge$_{0.2}$/Si are crucial factors in obtaining good performance. In the simulation, the steep junction below 13.2 degrees was used for better comparison of the structural aspects.

### 3 Junction profile and device fabrication

In order to investigate the cell characteristics of the proposed device structure, we performed an evaluation on the fabricated device. Fig. 3a shows a schematic of the junction device with a pattern size of $4 \times 4 \mu$m$^2$. Here, the strained N+ (Si$_{0.8}$Ge$_{0.2}$)/P (Si)/N+ (Si$_{0.8}$Ge$_{0.2}$) epitaxial layers are formed on the Si substrate. We selected a germanium composition of 20% because of its low dislocation [5]. The N+/P/N+ multilayer was formed using the Ultra High Vacuum Chemical Deposition (UHV-CVD) method. An in situ doped epitaxial SiGe and Si process was used to deposit at low temperature (< 600 °C). Fig. 3b shows the doping profile for this junction device, obtained by SIMS measurement. We confirmed the basic I-V characteristics under the heterojunction conditions.

As shown in Fig. 3b, the flat doping profiles of the N+ SiGe layer with $2 \times 10^{20}$ atoms/cm$^3$ and the P Si layer with $2 \times 10^{19}$ atoms/cm$^3$ were formed respectively. Moreover, a steep junction profile with 20~30 nm at the interface of Si$_{0.8}$Ge$_{0.2}$/Si was also confirmed. Here, the length of the P type Si layer was 50 nm.
After the doping experiment, the N+/P/N+ junction device with an area of $4 \times 4 \mu m^2$ was fabricated by photolithography. The patterned photo-resistor was used as a hard mask, and the SiGe and Si layers were etched by reactive ion etching (RIE). PECVD SiO$_2$ was deposited for isolation. Via was patterned by photolithography followed by SiO$_2$ RIE. The metal contact (Au/Ti: $2 \times 2 \mu m^2$) was fabricated by the lift-off technique, as in Fig. 3a.

Fig. 2. Simulation results for I-V characteristics under the junction structures of the proposed junction device.

a. I-V characteristics for Si$_{0.8}$Ge$_{0.2}$/Si (15/18/20 nm)/Si$_{0.8}$Ge$_{0.2}$

b. Doping profile of the Si$_{0.8}$Ge$_{0.2}$/Si interface with different slopes

c. I-V characteristics dependence on the doping slope
4 Device characteristics and discussion

Fig. 4 shows the result of the I-V measurement with the applied voltage ($-4$ V to $4$ V) using Agilent/HP 8110A Pulse Generation for the hetero-junction device with $4 \times 4 \text{um}^2$ areal. As shown in Fig. 4, we confirmed the bidirectional

Fig. 3. These figures show the experimental result for the N+/P/N+ bidirectional switching diode.

a. SIMS data: Doping profile density is $7 \times 10^{19}/2 \times 10^{19}/2 \times 10^{20}$ in the N+ (33 nm)/P (50 nm)/N+ (130 nm) layers, respectively

b. Top-view image of the fabricated device structure

Fig. 4. I-V characteristics of the fabricated switching diode using Agilent/HP 8110A Pulse Generation (applied voltage $-4$ V to $4$ V).
current flow. However, we found a low on-current density of about 0.05 MA/cm² at 3 V and a low $I_{on}/I_{off}$ ratio of below $10^3$ at an operational voltage range of less than 3 V. We understand that these characteristics result from differences with the optimal structural and doping conditions, which is proposed by device simulation. Therefore, further research is needed for the realization of a heterojunction device with the simulation conditions.

5 Conclusion

We proposed a novel heterojunction device with N+ Si$_{0.8}$Ge$_{0.2}$/P Si/N+ Si$_{0.8}$Ge$_{0.2}$, and presented optimal conditions for its realization with a current density of 1 MA/cm² and an $I_{on}/I_{off}$ ratio of more than $10^4$ by simulation, which is acceptable for an STT-MRAM. Moreover, flat and steep junction profiles were demonstrated in the doping experiment. And, we confirmed a bidirectional current flow from the I-V characteristics of the fabricated sample. From these results, we expect that a two terminal N+/P/N+ SiGe heterojunction structure could provide a solution as a bidirectional switching device for an STT-MRAM.

Acknowledgments

The authors would like to thank S.C. Oh of Samsung Electronics for his support and helpful discussions. This research was supported by the Ministry of Science, ICT & Future Planning (MSIP), Korea, under the Information Technology Research Center (ITRC) support program (NIPA-2014-H0301-14-1017) supervised by the National IT Industry Promotion Agency (NIPA).