Embedded current amplifier compensation for three-stage amplifiers with large capacitive loads

Pengfei Liao\textsuperscript{1a)}, Weizhong Chen\textsuperscript{2}, Ping Luo\textsuperscript{3}, and Luncai Liu\textsuperscript{1}

\textsuperscript{1} Analog IC Design Department, Acoustoelectric and Optoelectronic Corp.,
China Electronics Technology Group Corporation, Chongqing 400060, P. R. China

\textsuperscript{2} School of Electronic Engineering, Chongqing University of Posts and
Telecommunications, Chongqing 400065, P. R. China

\textsuperscript{3} State Key Laboratory of Electronic Thin Films and Integrated Devices,
University of Electronic Science and Technology of China,
Chengdu, 610054, P. R. China

\textsuperscript{a)} fly5221@gmail.com

Abstract: An embedded current amplifier compensation (ECAC) for three-stage amplifiers with large capacitive loads is presented in this paper. Two current amplifiers are embedded into the first stage. The compensation capacitor is connected to the input of the current amplifier rather than the output of the first stage, which enables the non-dominant complex poles of the ECAC amplifier to be located at high frequencies for bandwidth extension; in addition, the compensation capacitor required is greatly reduced. The amplifier has been fabricated in a 0.13 µm CMOS process. When driving a 2000 pF capacitive load, the ECAC amplifier achieves 1.85 MHz gain-bandwidth product by dissipating 33.6 µW power at 1.2 V supply and using total compensation capacitance of only 0.8 pF.

Keywords: current amplifier, capacitive load, compensation capacitor

Classification: Integrated circuits

References


1 Introduction

Operational amplifier, as a key module, is widely used in various analog and mixed-signal systems. Some applications, such as LCD driver, analog filter, demand low power amplifier that is capable of driving large capacitive loads up to nF-range [1, 2]. Compared to two-stage amplifier, three-stage amplifier has attracted much attention due to its high gain, wide output swing, especially the capability of driving capacitive loads. Even so, most of the chip area is occupied by the compensation capacitors in large-capacitive-load amplifier [3]. So various frequency compensation strategies [1, 3, 4, 5, 6, 7, 8, 9, 10] are developed to reduce compensation capacitor and lower the power consumption.

In [1, 4, 5], an active left-half-plane zero is generated to extend the load drivability, yet extra integrated resistor and two compensation capacitors are required. The compensation technique presented in [8] can drive ultra-large capacitive load with a small compensation capacitor, yet the systematic offset voltage incurs due to the asymmetry of the first stage.

This letter presents an embedded current amplifier compensation (ECAC) strategy, which only requires a small compensation capacitor to drive large capacitive load. The current amplifier is embedded into the first stage, the system offset is thus minimized. In addition, it offers significant technical merits in term of small-signal and large-signal performance metrics. This paper is organized as follows. The topology, transfer function, stability and circuit implementation of the proposed ECAC are described in Section 2. The results and discussions are presented in Section 3. Finally, the conclusion of this paper is given in Section 4.

2 ECAC amplifier

2.1 Topology

The topology of the ECAC amplifier is shown in Fig. 1. Both the second and third stages are inverting gain stages, which typically consume less power than non-inverting gain stages to achieve the same magnitude of transconductance. $k$ is the gain factor of the current amplifier $X_1, X_2$, which are embedded in the first stage. $g_{m1-3}$ and $R_{1-3}$ denote the transconductance and the output resistance of each stage, respectively. $C_f, C_{1-3}$ symbolize the lumped parasitic capacitance and $C_L$ is the load capacitor. $C_m$ is the key miller capacitor, accomplishing the frequency compensation. The key compensation capacitor is connected to the input of the
current amplifier, rather than the output of the first stage, therefore, the proposed ECAC does not suffer from the bandwidth reduction due to the presence of the right half zero. The feedforward stage \(g_{m2}\), along with the last stage form a pull-push stage to improve the large-signal performance. Furthermore, both the feedback signal through the \(C_m\) and the input signal are magnified by the current amplifier, the non-dominant poles can be pushed to higher frequencies, which results in enhanced capacity of driving capacitive load.

2.2 Transfer function

Follow the usual assumptions in three-stage amplifier [11], the transfer function of the ECAC amplifier can be calculated as

\[
A_v \approx \frac{A_{dc}\left(1 + \frac{sC_m}{2g_{m0}}\right)(1 + sR_fC_f)
\left(1 + s^2\frac{g_{m1}g_{m3}C_1C_f + g_{m2}g_{ma}C_1C_2}{kg_{m2}g_{ma}C_f}
- \frac{s^2g_{m1}C_1C_2}{kg_{m1}g_{m2}g_{m3}}\right)
}{\left(1 + \frac{1}{p-3dB}\right)^2
\left(1 + s^2\frac{C_1C_2}{kg_{m2}R_2g_{m3}C_m}
+ \frac{s^2C_1}{kg_{m2}R_2g_{m3}g_{ma}}\right)(1 + sR_fC_f)(1 + sR_2C_2)}
\]

(1)

Where \(A_{dc} = kg_{m1}g_{m2}g_{m3}R_1R_2R_3\) is the DC gain and the dominant pole is \(-p_{-3dB} = -1/(kg_{m2}g_{m3}R_1R_2R_3C_m)\). The gain-bandwidth product (GBW) is then obtained as

\[
GBW = A_{DC} \times |p_{-3dB}| = \frac{g_{m1}}{C_m}
\]

(2)

It is worth noting that, the dominant pole is pushed to lower frequencies due to the embedded current amplifier, however, the GBW achieved is not reduced as a result.

2.3 Stability

As shown in (1), a zero-pole pair \((p = z = 1/R_fC_f)\) exists due to the feedforward stage. It is clear that they are always equal to each other, which yields complete cancellation of this zero-pair pair. In addition, the zeros determined by the polynomial of the numerator

\[
1 + s^2\frac{g_{m1}g_{m3}C_1C_f + g_{m2}g_{ma}C_1C_2}{kg_{m2}g_{ma}g_{ma}C_f}
- \frac{s^2g_{m1}C_1C_2}{kg_{m1}g_{m2}g_{m3}}
\]

(3)

and the parasitic related pole \(o_p = -1/(R_2C_2)\) are located at high frequencies and their effects can be safely ignored [6].

Fig. 1. Topology of the proposed ECAC amplifier
Based on the analysis above, the transfer function shown in (1) can be simplified as

\[
A_v \approx \frac{A_{dc}}{1 + s C_25 A_{dc}} \left(1 + \frac{s}{C_18} \right) \left(1 + s C_m \frac{C_L C_1}{k g_{m2} R_{g_m3} g_{m3}} \right) \left(1 + s \frac{C_L C_1}{k g_{m2} R_{g_m3} g_{m3}} \right)
\]  

(4)

The position of the non-dominant complex poles can be derived as

\[
|p_{nd}| = \sqrt{\frac{k g_{m2} R_{g_m3} g_{m3}}{C_L C_1}}
\]  

(5)

By embedding the current amplifier in the first stage, the position of non-dominant complex poles is pushed to much higher frequencies than that of the structure proposed in [3], meanwhile the dominant pole is pushed to lower frequencies, in other words, the pole-splitting is more evident and stability of the ECAC amplifier is guaranteed. Apply the low-power stability strategy in [12], the dimension condition of the compensation capacitor is calculated as

\[
C_m = \sqrt{\frac{1.5 g_{m1} C_L C_1}{k g_{m2} R_{g_m3}}}
\]  

(6)

As shown in (6), the value of the compensation capacitor is inverse proportional to the square root of the product of \(k\) and the gain of the second stage. It can thus be significantly reduced through suitable choice of \(k\) and the gain of the second stage, which implies that the GBW, slew rate (SR) and power-efficiency of the ECAC amplifier can be further enhanced by using the proposed compensation strategy.

2.4 Circuit implementation

The circuit implementation of the ECAC amplifier is shown in Fig. 2. The first stage is realized by transistors \(M_{0-10}\) with a PMOS input differential pair. The current amplifiers composed of \(M_{3-4}\) and \(M_{5-6}\) are embedded in the first stage without extra bias circuits. The first stage is full symmetry so the system offset is obviously minimized compared to active-feedback compensation [1, 5]. The second stage is a common-source amplifier composed of \(M_{11-12}\), \(M_{12}\) serves as the feedforward stage \(g_{m1}\). The output stage is composed of a feedforward stage \(g_{m2}\) and the third gain stage, forming the pull-push stage \(g_{m3}\). The feedforward stage

![Fig. 2. Circuit implementation of the proposed ECAC amplifier](image-url)
$g_{\text{m}2}$ is realized by $M_{18}$, whereas the third gain stage is realized by NMOS $M_{17}$. The compensation network is constituted of $C_m$ and current amplifier composed of $M_{3-4}$. The load capacitance $C_L$ is taken to be 2000 pF and a compensation capacitance $C_m$ of only 0.8 pF is used to stable the ECAC amplifier. The total current consumption is only 28 µA.

3 Results and discussions

To verify the validity of the proposed compensation strategy, the ECAC amplifier is designed and simulated in different corners. Post-layout simulation results shows that, even in the worst speed corner (SS), the DC gain is over 100 dB and the GBW is 1.85 MHz with phase margin of 52°, which is shown in Fig. 3.

The proposed ECAC amplifier is implemented in a 0.13 µm standard CMOS process and the microphotograph is shown in Fig. 4. The area is 0.09 * 0.062 mm², which is relatively small due to the small compensation capacitor.

The measured step response of the ECAC amplifier is shown in Fig. 5 and the average slew rate (SR) is 0.22 V/µs. The total current consumption is only 28 µA.

To evaluate the performance of different amplifiers, besides the traditional two reasonable figures of merit (FOM), $\text{IFOM}_S = (\text{GBW} \cdot C_L / I_{dd})$ and $\text{IFOM}_L = (\text{SR} \cdot C_L / I_{dd})$, two novel FOM, $\text{LC-IFOM}_S = (\text{GBW} / I_{dd})$ and $\text{LC-IFOM}_L = (\text{SR} / I_{dd})$ are used to characterize the small-signal (GBW) and large-signal (slew
rate) capabilities including area-efficiency. Key parameters and performance comparison are given in Table I. Obviously, the ECAC is an area-efficiency frequency compensation strategy for large capacitive load.

4 Conclusion
A novel compensation strategy for three-stage amplifier is proposed in this paper. By means of embedding current amplifier in the first stage, it can drive 2 nF capacitive load with a compensation capacitor of only 0.8 pF, which indicates the proposed compensation strategy is an area-efficiency for large capacitive load.

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