A digitally enhanced LDO voltage regulator for UHF RFID passive tags

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Abstract: This work proposes a Digitally Enhanced Low-Drop Out Voltage Regulator (DE-LDO) for Ultra High Radio Frequency IDentification (UHF RFID) passive tags. The DE-LDO design approach is based on the Finite State Machine (FSM) nature of the tag Digital Control. Injecting part of the FSM unconsumed current into LDO loop to enhance transient response, a more flat output voltage is obtained. Chip measurements shows that DE-LDO consumes a quiescent current of 600 nA at 1.6 V, delivering an output current and voltage of 8 μ A and 1.2 V; a 69.76% Power Efficiency (PE) is observed. Circuit design and fabrication were performed using 0.50 μ m CMOS technology.

Keywords: UHF RFID, passive tag, LDO voltage regulator, phase margin, GBW, digital control, finite state machine

Classification: Integrated circuits

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1 Introduction

Ultra High Radio Frequency IDentification (UHF RFID) has been in the market around forty years since its first apparition as replacement of the bar code technology, [1]. However, due to its versatility, new applications were shown up across the time like access control, personal and animal tracking, storage, network monitoring and, the newest one, physical variable monitoring, [2]. RFID system is build by three major elements: reader, Radio Frequency (RF) link and tag, Fig. 1a. The reader emits a RF energy, called down-link, that contains Amplitude Shift Keying (ASK) digitally modulated data. The tag uses the down-link to extract digital data as well as DC energy to supply its circuitry, activating the digital control. The tag responds to the reader via backscatter modulation changing its antenna reflection coefficient. The reader senses and decodes the small voltage fluctuations at its antenna caused by the reflected wave as tag’s response, [3].

Fig. 1. RFID system

The new passive tags are made up by five building blocks: transducer, power management, transceiver, digital control and ADC/sensor, Fig. 1b. Transducer block is composed by an antenna and a matching network. The antenna transforms electric fields into a voltage difference at its terminals while the matching network ensures maximum power transfer from the antenna to the rectifier. Rectifier, band

gap and voltage regulator built the power extraction block. Rectifier circuit generates a DC component from the energy delivered by the matching network. However, as the available power in the media depends on the relative separation distance between the reader and the tag, it is expected that the rectifier output voltage present large ripples. The correct operation of the digital control can not be ensured if it is directly supplied by the rectifier output, the insertion of a voltage regulator must be considered. The voltage regulator, typically a Low-Drop Out Voltage Regulator (LDO), provides a stable DC level to the digital control under line and load modulations. Currents and voltages references to bias subsequent analog sections are generated in the band gap block. The required protocol or standard needed to establish a communication link is stored in the digital control, which also controls the Analog-Digital Converter (ADC) number of samples per instruction needed to gather a correct measure of a certain physical variable from the sensor. The transceiver stage is made up by an ASK demodulator and backscatter modulator. The demodulator extracts the digital envelope from the RF link and recovers its logic voltage levels. Backscatter modulator receives digital data coming from the digital control and generates a proportional change in the reflection coefficient of the tag's antenna, [4, 5, 6, 7].

Intensive research has been focused on UHF RFID LDO trying to decrease quiescent current consumption while keeping fast transient response. The work presented in [8] makes use of a Miller compensated error amplifier and pole-zero cancellation technique to ensure stability under load modulations. In [9], diode-like PMOS transistor are used as replacement of resistors located at LDO's loop, providing higher resistance values saving silicon area and decreasing the feedback loop current consumption. In order to increase the line modulation factor, [10] makes use of a ripple and temperature stabilizer. Due to GBW parameter plays a major role in load modulation response, the work presented in [11] boosts the tail current of the error amplifier in the LDO, improving the GBW as well as load modulation.

This work presents a new Digitally Enhanced Low-Drop Out Voltage Regulator (DE-LDO) design approach based on the ability to predict the average power consumption of the tag digital control. This prediction can be done due to digital control main core is a Finite State Machine (FSM). Using this approach a less variant load at the RF-harvesting output is observed as well as a more flatten output voltage delivered by the DE-LDO.

This work is organized as follows. Section II presents the analysis, basis and circuit implementation of the proposed DE-LDO. Experimental results are provided in Section III. Conclusions are given in Section IV.

2 Basis and circuit implementation

As mentioned in previous section, the DC power needed to turn on the RFID passive tag is extracted via low-threshold RF harvesters whose design methodology assumes a constant load attached at their output. However, this design methodology is not entirely truth due to tag digital core shows different current consumption ratios at different times. Another RFID passive tag essential building block affected

by this current consumption variation is the LDO, modifying its ability to deliver a flat output voltage to the tag digital control.

Tag digital control current consumption is mainly governed by the state in which its FSM is, [12]. Because of FSM follows a stated/conditioned sequential path, the power consumption of the previous and next state can be predicted. By knowing the power consumption in each state of the tag digital control, the LDO transient response can be digitally enhanced by injecting back the digital control unused current into LDO feedback loop. This digital enhancement improves RFID passive tags in two ways. The first improvement is shown at LDO output, delivering a more flat supply voltage to the digital control avoiding unknown states and processing errors. The second improvement helps to keep a less-variant load at the RF harvesting; the PCE efficiency is now only affected by reader-to-tag separation distance and input power but consumed power.

2.1 Digitally enhanced low-drop out voltage regulator design

The proposed Digitally Enhanced LDO Voltage Regulator (DE-LDO) is shown in Fig. 2. In order to simplify LDO stability analysis, the dashed line block called Digital Enhancement is omitted. Stability criteria is accomplished via placing an Indirect Miller compensation capacitor C_{mos} between the low impedance node provided by node V_X and V_{OUT_LDO} . Capacitor-like PMOS transistor was implemented due to smaller silicon area consumption compared with poly-poly2 capacitors.

Fig. 2. Digitally enhanced LDO voltage regulator

The small-signal model of the proposed LDO is presented in Fig. 3. In order to obtain its transfer function the following assumptions were done: $g_{mp01} \cong g_{mp02} \cong g_{mp03} \cong g_{mp04} \cong g_{mp}$, $g_{mn1} \cong g_{mn2} \cong g_{mn}$, $R_x = \frac{1}{g_{mploop}} \parallel R_L \parallel r_{opass}$ and $g_{mk}r_{ok} \gg 1$, where g_{mnk} , g_{mpk} and r_{ok} are the transconductances of the k-th transistor and k-th channel resistance. C_{gdpass} and g_{mpass} corresponds to m_{pass} gate-drain capacitance and transconductance. The obtained transfer function has the form of (1), where A_v is the DC gain, $N(s)$ and $D(s)$ are second and third order polynomials. DC gain A_v , $N(s)$ and $D(s)$ are shown in (2), (3), (4), respectively.

Fig. 3. LDO voltage regulator small signal model

$$FT_{loop}(S) = Av \frac{N(s)}{D(s)} = Av \frac{A_z s^2 + B_z s + 1}{A_p s^3 + B_p s^2 + C_p s + 1} \quad (1)$$

$$Av = -g_{m_n} r_{o_n} g_{m_{pass}} R_x \quad (2)$$

$$N(s) = -\frac{C_{mos} C_{gd_{pass}}}{g_{m_p} g_{m_{pass}}} s^2 - 2C_{mos} r_{o_n} r_{o_p} g_{m_{pass}} s + 1 \quad (3)$$

$$D(s) = \frac{C_{mos} C_{gd_{pass}} (C_{mos} + C_L) r_{o_n} R_x}{g_{m_p}} s^3 + \dots$$

$$\dots + \left\{ C_{gd_{pass}} r_{o_n} R_x \left[C_L + C_{mos} \frac{g_{m_{pass}}}{g_{m_p}} \right] + C_{mos} \frac{R_x}{g_{m_p}} (C_{mos} + C_L) \right\} s^2 + \dots$$

$$\dots + R_x [C_L + C_{mos} + C_{gd_{pass}} r_{o_n} g_{m_{pass}}] s + 1 \quad (4)$$

Equation (1) suggest a two zero numerator and a three pole denominator whose locus directly varies with the load magnitude. From equation (3), ω_{z0} and ω_{z1} zero location can be computed into (5) and (6). ω_{z0} zero is added by C_{mos} indirect Miller compensation capacitor and it is placed at the left side of the $j\omega$ plane. ω_{z1} is added by $C_{gd_{pass}}$ capacitor and it is placed at the right side of the $j\omega$ plane. Fig. 4a shows zero movement in the $j\omega$ plane as function of delivered current to the load.

$$\omega_{z0} = -\frac{1}{2C_{mos} r_{o_n} r_{o_p} g_{m_{pass}}} \quad (5)$$

$$\omega_{z1} = \frac{2r_{o_n} r_{o_p} g_{m_p} g_{m_{pass}}^2}{C_{gd_{pass}}} \quad (6)$$

Fig. 4. Zero movement

The denominator presented in (4) is analyzed under no-load, medium-load and full-load. In the first scenario, no-load conditions allows $C_L \gg C_{mos} \frac{g_{m_{pass}}}{g_{m_p}}$ and

$(C_L + C_{mos}) \gg C_{gd_{pass}} r_{on} g_{m_{pass}}$ to be assumed, modifying (4) into (7). No-load condition, suffix *NL*, leads to a completely separated poles. The dominant pole is located at much lower frequencies than the first non-dominant pole. Locus of the dominant pole $\omega_{p0_{NL}}$, first non-dominant pole $\omega_{p1_{NL}}$, second non-dominant pole $\omega_{p2_{NL}}$ and GBW_{NL} are given by (8), (9), (10) and (11), respectively. Dominant pole $\omega_{p0_{NL}}$ depends on the load current, $R_x \propto I_{LOAD}$, and load capacitor C_L . First non-dominant pole $\omega_{p1_{NL}}$ is governed by the Indirect Miller Capacitor C_{mos} .

$$D(s) = \frac{C_{mos} C_{gd_{pass}} (C_{mos} + C_L) r_{on} R_x}{g_{m_p}} s^3 + \dots$$

$$\dots + R_x \left[C_{gd_{pass}} C_L r_{on} + \frac{C_{mos}}{g_{m_p}} (C_{mos} + C_L) \right] s^2 + R_x (C_L + C_{mos}) s + 1 \quad (7)$$

$$\omega_{p0_{NL}} = - \frac{1}{R_x (C_{mos} + C_L)} \quad (8)$$

$$\omega_{p1_{NL}} = - \frac{g_{m_p}}{\frac{C_{gd_{pass}} C_L r_{on} g_{m_p}}{C_{mos} + C_L} + C_{mos}} \quad (9)$$

$$\omega_{p2_{NL}} = - \left\{ \frac{1}{C_{gd_{pass}} r_{on}} + \frac{C_L}{C_{mos}} \frac{g_{m_p}}{C_{mos} + C_L} \right\} \quad (10)$$

$$GBW_{NL} = \frac{g_{m_n} r_{on} g_{m_{pass}}}{C_{mos} + C_L} \quad (11)$$

Medium load condition, suffix *ML*, is applied on (4) when the level of current through M_{pass} begins to be significant increasing $g_{m_{pass}}$ value. Under this case only $C_L \ll C_{mos} \frac{g_{m_{pass}}}{g_{m_p}}$ assumption can be applied, modifying (4) into (12). The dominant pole still being at much lower frequency than the first non-dominant pole, allowing a widely separate poles. The locations of the dominant pole $\omega_{p0_{ML}}$, first non-dominant pole $\omega_{p1_{ML}}$, second non-dominant pole $\omega_{p2_{ML}}$ and GBW_{ML} are given by (13), (14), (15) and (16), respectively. As can be seen, the dominant pole $\omega_{p0_{ML}}$ is shifted by a $C_{gd_{pass}} r_{on} g_{m_{pass}}$ factor that is directly proportional to the load current, $g_{m_{pass}} \propto I_{LOAD}$. First no-dominant pole $\omega_{p1_{ML}}$ remains governed by the Indirect Miller Capacitor C_{mos} .

$$D(s) = \frac{C_{mos} C_{gd_{pass}} (C_{mos} + C_L) r_{on} R_x}{g_{m_p}} s^3 + \dots$$

$$\dots + C_{mos} \frac{R_x}{g_{m_p}} (C_{gd_{pass}} r_{on} g_{m_{pass}} + C_L + C_{mos}) s^2 + \dots$$

$$+ R_x (C_{gd_{pass}} r_{on} g_{m_{pass}} + C_L + C_{mos}) s + 1 \quad (12)$$

$$\omega_{p0_{ML}} = - \frac{1}{R_x (C_{mos} + C_L + C_{gd_{pass}} r_{on} g_{m_{pass}})} \quad (13)$$

$$\omega_{p1_{ML}} = - \frac{g_{m_p}}{C_{mos}} \quad (14)$$

$$\omega_{p2_{ML}} = - \left\{ \frac{1}{C_{gd_{pass}} r_{on}} + \frac{g_{m_{pass}}}{C_{mos} + C_L} \right\} \quad (15)$$

$$GBW_{ML} = \frac{g_{m_n} r_{on} g_{m_{pass}}}{C_{mos} + C_L + C_{gd_{pass}} r_{on} g_{m_{pass}}} \quad (16)$$

Full load condition, suffix FL , leads to a first and second non-dominant complex conjugated poles. In this operation regime the dominant pole $\omega_{p0_{FL}}$ and GBW_{FL} still being given by (13) and (16) although dominant pole $\omega_{p0_{FL}}$ is shifted due to $g_{m_{pass}}$ reaches its maximum value. If $\omega_{p0_{FL}}$ is extracted from the denominator (12), a new second order denominator is obtained. This new denominator can be solved via quadratic equation. If the condition of $b^2 < -4ac$ in the determinant of the quadratic equation is accomplished, complex conjugated poles are obtained. The location of $\omega_{p1_{FL}}$ and $\omega_{p2_{FL}}$ is given by (17). Fig. 4b shows how pole locations is changed as function of the load current. LDO Power Efficiency (PE) is calculate by (18).

$$\omega_{p1,2_{FL}} = -\frac{1}{2} \left\{ \frac{1}{C_{gd_{pass}} r_{on}} + \frac{g_{m_{pass}}}{C_{mos} + C_L} \right\} \pm \sqrt{\frac{g_{m_p}}{C_{mos}} \left[\frac{1}{C_{gd_{pass}} r_{on}} + \frac{g_{m_{pass}}}{C_{mos} + C_L} \right]} \quad (17)$$

$$PE = \frac{I_{out_{LDO}} V_{out_{LDO}}}{(I_{out_{LDO}} + I_{quiescent}) V_{in_{LDO}}} * 100\% \quad (18)$$

2.2 Digital enhancement

As it was explored in the previous section, pole and zero locus varies according with the load current, which also affects the transconductance $g_{m_{pass}}$ of the pass element modifying the Phase Margin (PM) and the Gain Band-Width (GBW) parameters. LDO transient response and its ability to deliver a flat output voltage is set by its open loop bandwidth as shown equation (19). Digital Enhanced technique helps to keep the load current value close enough to operate the pass element $m_{p_{pass}}$ always in saturation regime, minimizing the fluctuations in PM and GBW. According with the small signal in Fig. 3, the load is modeled as an equivalent resistor R_X , (20), where the only parameter that can be controlled in order to keep the magnitude of R_X constant is the value of $\frac{1}{g_{mp_{loop}}}$. If the magnitude of R_L increases, $\frac{1}{g_{mp_{loop}}}$ should decrease and vice-versa.

$$\omega_{-3dB} = (1 + \beta A_{OL})_{-3dB} \cong \beta GBW \quad (19)$$

$$R_X = \frac{1}{g_{mp_{loop}}} \| R_{LOAD} \| r_{o_{pass}} \quad (20)$$

In Fig. 2 the Digital Enhancement is implemented via five diode-like PMOS transistors, mp05–mp09, whose job is acting like parallel resistor with mp_{loop} , modifying the current in the LDO feedback loop. These parallel resistors are activated by a five-bit word with the aim of NMOS transistors mn04–mn08 that act as linear switches. The amount of current injected back to the LDO feedback loop corresponds to the unused current by the tag Digital Control depending on the state in which the FSM is.

3 Measurements and results

Fig. 5 shows CAD designed and fabricated layout used to perform typical LDO and DE-LDO measurements, characterization and comparisons; silicon area consumption is $600 \mu m \times 190 \mu m$. In order to characterize both LDOs, a digitally

programmed current sink was implemented with the aim of commercially available ALD1106-NMOS, ALD1107-PMOS, and a prototyping board Digilent-Explorer. Such current sink is used to emulate tag digital control current consumption but also provides necessary the control-command bits to inject back into the LDO feedback loop the unused current, increasing LDO transient response. Table I shows the current load assumptions per each state of the FSM, I_{LOAD} , the control bit command to inject the unused current into LDO feedback loop, BIT , the amount of injected current into the loop, I_{LOOP} , and the total current through $m_{p_{pass}}$, $I_{m_{p_{pass}}}$.

Fig. 5. Proposed DE-LDO layout and micro-photographic

Table I. Digital control sequence

State	I_{LOAD}	BIT	I_{LOOP}	$I_{m_{p_{pass}}}$
<i>Arbitrate</i>	8.00 μ A	00000	0.3 μ A	8.3 μ A
<i>Replay</i>	6.66 μ A	00001	0.6 μ A	7.26 μ A
<i>Acknowledged</i>	5.33 μ A	00011	0.9 μ A	6.23 μ A
<i>Open</i>	4.00 μ A	00111	1.2 μ A	5.2 μ A
<i>Secured</i>	2.66 μ A	01111	1.5 μ A	4.16 μ A
<i>Killed</i>	1.33 μ A	11111	1.8 μ A	3.13 μ A

Fig. 6 presents the transient response under no-load and full-load condition, subplots a) and b) corresponds to typical-LDO while c) and d) resembles DE-LDO. Comparing Fig. 6a and Fig. 6c where LDO input voltage is $V_{DD} = 1.6$ V, it can be seen a ripple reduction from ± 40 mV in typical-LDO to ± 10 mV in DE-LDO during no-load. However, voltage overshoots of 220 mV and 368 mV for typical-LDO and DE-LDO, respectively, during no-load to full-load transition are observed; such behavior does not degrades DE-LDO performance due to this test-bench only emulates the tag digital control turning-on and turning-off. A LDO input voltage of $V_{DD} = 1.8$ V is used in Fig. 6b and Fig. 6d showing the same behavior, ripple voltage during no-load state are decreased from ± 40 mV to ± 5 mV using DE-LDO but voltage is increased from 240 mV to 448 mV.

Fig. 6. Transient response under no-load and full-load conditions for typical-LDO, a) and b), and DE-LDO, c) and d).

Figs. 7 and 8 shows different load current test-benches. Fig. 7 uses a 1.33 μA continuous steps from full-load to no-load current conditions, while Fig. 8 implements an no-load to ever-increasing 1.33 μA current steps. From Figs. 7 and 8, two

Fig. 7. Transient response under 1.33 μA continuous steps from full-load to no-load conditions for typical-LDO, a) and b), and DE-LDO, c) and d).

observations can be established: DE-LDO decreases in a 60% output voltage ripples and overshoots are also decreased during small current step changes.

Fig. 8. Transient response under no-load to ever-increasing 1.33 μ A steps conditions for typical-LDO, a) and b), and DE-LDO, c) and d).

4 Conclusion

A Digitally Enhanced Low-Drop Out Voltage Regulator (DE-LDO) suitable for UHF RFID passive tags was proposed and discussed. A Digital Enhancement mechanism based on feeding back the unconsumed tag Digital Control current into the DE-LDO feedback loop was used. Such approach helped to keep a semi constant load at RF-Harvester output. Chip measurements showed a more flat output voltage provided by DE-LDO, compared with typical LDO. The proposed DE-LDO quiescent current and voltage consumption were 600 nA at 1.6 V. An output current and voltage of 8 μ A and 1.2 V were provided to the load. A DE-LDO power efficiency of 69.76% was achieved. Circuit design and fabrication were performed using 0.50 μ m CMOS technology.

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