An efficient digital calibration technique for timing mismatch in time-interleaved ADCs

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Abstract: An efficient digital calibration technique for timing mismatch in time-interleaved ADCs is presented. It depends on the phase detection between a reference clock and the sampling clock of each sub-ADC in TIADC system. A method of variable delay line is used to compensate the timing mismatch. The mismatch detection and compensation form a feedback loop and can achieve a real-time tracking and correcting. Simulation results showed that this technique can have the timing mismatch calibrated quickly and correctly within the entire Nyquist sampling frequency by the virtue of a smaller hardware, and can be applied to any number of TIADC.

Keywords: time-interleaved ADC, timing mismatch, error estimation, error compensation

Classification: Electron devices, circuits and modules

References
1 Introduction

Due to the variations in manufacturing process technology, there are a variety of mismatches between channels of time-interleaved ADCs (TIADCs), and these mismatches can greatly degrade the ADC’s performance [1, 2]. Among them, the mainly three mismatches are offset mismatch, gain mismatch and timing mismatch. The offset and gain mismatch introduce DC terms and gain product terms respectively [3], which can be easily calibrated by adders and multipliers. But the timing mismatch is relatively difficult to calibrate due to its complex detection and correction, and has become the focus of research today. A number of recent studies have been conducted on timing mismatch mitigation, however, they still have many shortcomings, like limited by the number of channels [4, 5], limited by bandwidth of the input signal [6], high hardware consumption [7, 8], or slow calibration speed [9].

In order to overcome the drawbacks of the existing calibration techniques, this paper proposed an efficient calibration technique for timing mismatch in time-interleaved ADCs. This technique directly estimates and compensates the timing mismatch error in the sampling clock path, so it was not limited by number of channels and bandwidth of the input signal. The system clock is set as the reference clock signal, after calibration, the rising edge of all sub-ADC clocks can be aligned sequentially with the system clock. Error detection circuits use only D flip-flops, subtractions and logical selection units, and the hardware implementation is very simple. Error compensation is realized by a variable delay line, which is much fast and precise. Simulation results showed that this method can be applied to any number of channels and the calibration within the entire Nyquist sampling frequency by virtue of a smaller hardware.

2 Timing mismatch calibration

A block diagram of a TIADC is shown in Fig. 1(a), each sub-ADC alternately samples the analog input which is on the front-end and converts the analog signal into a digital signal, and then through a synthesis module converts the outputs of multiple channels into a digital output. Fig. 1(b) is the system clock schematic of TIADC. If the clock cycle of each channel ADC is $T_{\text{sub}}$, the sampling interval of the adjacent channel ADC is $T_s = T_{\text{sub}}/M$, and that the input signal sampling fre-
The frequency of TIADC system is \( f_s = M \cdot f_{sub} \) \( (f_s = 1/T_s, f_{sub} = 1/T_{sub}) \), which increases M-fold relative to the single channel ADC.

However, the performance of TIADCs is sensitive to the channel mismatches, which will cause spurious spectrum and degrade the signal-to-noise ratio. Among different kinds of mismatches, the timing mismatch presents much more challenge due to its frequency dependent detection. The calibration scheme of the proposed timing mismatch is shown in Fig. 2. The calibration of the timing mismatch contains two steps: detection and compensation. Here, the sampling clock of the first channel is firstly calibrated by taking the system clock as a reference clock. When the clock of the first channel is calibrated, it can be considered as a reference clock to have the remaining sampling clock of TIADC calibrated. The detailed calibration principle is as follows.

### 2.1 Timing mismatch detection

To estimate the timing mismatch of the first channel clock, we use the system clock as a reference clock, and the detection scheme is shown in Fig. 3. For simplicity, we take a four-channel TIADC as example. It uses a counter to count the system clock for four times, and uses a selector switch to generate \( clk_1 \). Then the timing skew between \( clk_1 \) and \( clk_1 \_out \) can be estimated by using a subtractor and a D flip-flop. When there is a time mismatch in \( clk_1 \_out \), we can judge the direct of calibration by the different value of \( choose1 \) as shown in Fig. 4.

![Fig. 2. The system clock schematic for a M-channel TIADC with timing calibration.](image-url)
To estimate the timing mismatches of the remaining clock of TIADC, we take the calibrated first channel clock $clk_1$ as a reference clock. When there is no timing mismatch between channels, the adjacent channels exist a delay of $T_s$. If there is a timing mismatch error between channels, the time delay between channels will be uncertain. When calibrating the clock of i-channel, we have $clk_{i\_out}$ delayed $(i-1)T_s$ by D flip-flops, and do subtraction with the i-th channel clock. Then we use the D flip-flops and error determination module to get the timing mismatch error between the first channel and the i-th channel. The specific estimate schematic is shown in Fig. 5.

"Fig. 4. The choose1 caused by different time mismatch (a) $\Delta t > 0$. (b) $\Delta t < 0$."

"Fig. 5. Timing mismatch detection schematic."
clki\_out is the sampling clock of the i-th channel which needs to be calibrated. clk1\_delayi is realized by having clk1\_out delay \((i - 1)T_s\) cycles. If there is a timing mismatch error which is equal to \(\Delta t\) between clk1\_delayi and clki\_out, they will not be perfectly aligned. To detect the timing mismatch error, we have them subtracted and obtain outi. Ideally, when there is no timing mismatch error in clki\_out, outi will always be 0, but if there is a timing mismatch error, outi will be fluctuating between 1, 0 and −1, as shown in Fig. 6(a), (b), (c).

![Diagram](image-url)

**Fig. 6.** Result after subtraction. (a) \(\Delta t = 0\). (b) \(\Delta t > 0\). (c) \(\Delta t < 0\)

Then, the D flip-flop module and error determination module are used to detect the timing mismatch error. For the digital sampling module, the output signal outi is triggered by clk1\_delayi and clki\_out to get outi1 and outii respectively: if \(\Delta t > 0\), the output outi1 is 1 after outi is sampled by clk1\_delayi, and the output outii is 0 after outi is sampled by clki\_out; if \(\Delta t < 0\), the output outi1 is 0 after outi is sampled by clki\_out, and the outii is −1 after outi is sampled by clki\_out, which is shown in Fig. 7(a), (b).
For the error determination module, it analyzes the output signal $out_{i1}$ and $out_{ii}$ under different error sampling conditions, and obtains the output $choosei$ of the timing mismatch error. If $out_{i1} = 1$ and $out_{ii} = 0$, $choosei$ is equal to 1; if $out_{i1} = 0$ and $out_{ii} = -1$, $choosei$ is equal to $-1$; if $out_{i1} = 0$ and $out_{ii} = 0$, $choosei$ is equal to 0.

### 2.2 Timing mismatch compensation

About timing mismatch errors compensation section, we use a variable delay line way to have the error compensated [10], and the method has the advantage of high speed of calibration and high accuracy. Fig. 8 shows the variable delay line compensation principle. The changing of the delay of the inverter between input and output is realized by changing the source-level current of the inverter. Wherein, the size of the delay unit is determined by clock to meet the maximum jitter of TIADC and $V_1$ and $V_2$ is among VDD and GND. The compensation process is as follows. First, we have the $k_L$ ($2 \leq L \leq n - 1$) switch closed, and the rest of the switches are in the off state, which means that always only one switch is closed. When $choosei = 1$, the closed switch will be $k_{L-1}$, which means that signal clk}

![Fig. 7. The output $out_i$ is sampled by clk1.delayi and clk1.out.

(a) $\Delta t > 0$. (b) $\Delta t < 0$.](image1)

![Fig. 8. The compensate schematic based on a variable line.](image2)
reduce a unit of delay; when \( choose_{i} = -1 \), the closed switch will be \( k_{L+1} \), which means that signal clki increase a unit of delay; when \( choose_{i} = 0 \), the closed switch will be unchanged. The switch judges every fixed time, and compensates the output clki.out gradually until it close to the ideal sampling clock of the i-th channel.

3 Simulation results

A behavioral model of a four-channel TIADC based on the proposed digital background calibration algorithm is designed and simulated in MATLAB. The sampling frequency of the TIADC is 1 GHz, and the designed resolution is 12 bits. For simplicity, the offset and gain mismatch are not be considered. The timing mismatch that adds into the TIADC behavior model is \( \Delta t = [-0.01T_s, 0.01T_s, 0.03T_s, -0.02T_s] \). With a normalized frequency of the input signal \( f_{in}/f_s = 0.48 \), Fig. 9 shows the output spectrum of the four-channel TIADC before and after calibration. It can be seen that the spurious spectrum due to the timing mismatch is very obvious before calibration with SNR only 25 dB. After calibration, the spurious spectrum is greatly disappeared, and SNR improves to 73 dB, ENOB enhances to 11.8 bits. Fig. 10 shows the convergence process of the timing mismatch. The timing mismatches reach their minimum in approximately \( 2 \times 10^3 \) samples. From Fig. 11, we can see that this method can be applied to the calibration within the entire Nyquist sampling frequency. Table I summarizes the performance of this work as well as other references, we can see this work using fewer adders and zero multiplier, and the convergence time is also the shortest among them.

![FFT Plot](a) before calibration (b) after calibration
4 Conclusion

This paper proposed an efficient technique for timing mismatch in time-interleaved ADCs. Compared with traditional calibration methods, this technique can quickly and easily get the timing mismatch error of each channel and compensate it for efficient. What’s more, it has a small hardware consumption and can be applied to any number of channels TIADC within the entire Nyquist sampling frequency. Applied to a 12 bit-1 GHz four-channel TIADC with the normalized frequency fin/fs = 0.48, simulation results showed that, after calibration, the SNR improved above 48 dB and ENOB enhanced 8 bits. The performance of TIADC was significantly improved, which proved the validity of the calibration technique.

Table I. Performance comparison

<table>
<thead>
<tr>
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<th>[6]</th>
<th>[7]</th>
<th>[9]</th>
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<td>Channels</td>
<td>16</td>
<td>4</td>
<td>4</td>
<td>4</td>
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<tr>
<td>Filter (taps)</td>
<td>/</td>
<td>31</td>
<td>/</td>
<td>/</td>
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<tr>
<td># of adders</td>
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<td>6</td>
<td>15</td>
<td>4</td>
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<td># of multipliers</td>
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<td>12</td>
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<tr>
<td>Convergence time (number of samples)</td>
<td>$2 \times 10^6$</td>
<td>$1.5 \times 10^7$</td>
<td>$1.6 \times 10^5$</td>
<td>$2.1 \times 10^3$</td>
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Fig. 10. Timing mismatch convergence time.

Fig. 11. The calibration effect of the method when the input frequency changes.