Design optimizations for a high-speed two-layer graphene optical modulator on silicon

Goran Kovacevic and Shinji Yamashita
Research Center for Advanced Science and Technology, University of Tokyo, 4–6–1 Komaba, Meguro-ku, Tokyo 153–8505, Japan
a) gorank@cntp.t.u-tokyo.ac.jp

Abstract: Graphene has emerged as one of the best novel materials for enhancement of various optical devices due to its exceptional light-matter interaction and optical properties. In this paper we focus on the integrated graphene optical modulator on a silicon waveguide, and show that by choosing specific design parameters of the device, we can achieve performances which surpass the previously reported graphene, and even all silicon modulators in speed, energy consumption and footprint. We substantiate our findings through numerical simulations and provide a deeper qualitative insight into the light matter interaction in graphene coated silicon waveguides.

Keywords: graphene, silicon waveguides, modulator, absorption

Classification: Integrated optoelectronics

References


1 Introduction

Graphene enhanced silicon photonics and optoelectronics has experienced an enormous expansion in the last couple of years, with various, highly efficient and compact integrated devices being proposed, like optical filters [1], modulators [2] and photodetectors [3, 4]. The main reason for the success of graphene are its exceptional optical properties [5] which perfectly complement the benefits of silicon photonics and enable creating ultra-small, and very energy efficient devices required for a sustainable usage in integrated photonics. The main issue with these novel hybrid devices, preventing them from being truly comparable with the all-silicon ones, is their weak response time and slow speeds, arising from large resistances occurring between graphene and the metal electrodes they have to use in operation, and large energy consumption. There has been some improvement in the device speeds of graphene based photodetectors and modulators recently [6, 7], but these structures are usually very difficult to fabricate and implement in larger systems.

In this paper, we propose advancements to the established two-layer graphene modulator on silicon [8] which include an asymmetric graphene capacitor structure and silicon waveguide design parameters optimization which maximizes the controllable, graphene induced absorption. Both of these novelties significantly increase the speed of the device (without adding to the complexity of the structure), and reduce its power consumption.

It is traditionally believed that the main way of improving the performance of graphene based modulators on silicon is through the improvements in the fabrica-
tion process. We prove through our design that there are still ways to optimize the standard device structures through pure electromagnetic reasoning. In fact, it is the belief of the authors of this paper that the graphene’s light matter interaction with the evanescent electromagnetic fields (as is the case of graphene coated silicon waveguides used in modulators) is still not fully explored, and that only through a better understanding of the underlying physical processes can we create truly optimal devices. Our novel modulator design is fundamentally based on some of the novel properties we discovered in the absorption curves of the graphene coated silicon waveguides, which we use in the silicon waveguide design optimization [9, 10].

We substantiate all our qualitative reasoning through numerical simulations. For the characterization of the graphene induced absorption in coated silicon waveguides we use a self-implemented graphene modified 2D FDM method [9] applied on the Maxwell's equations and we characterize the speed and the energy consumption of the proposed device through standard equations.

2 Optimizations of the two-layer graphene modulator on silicon

The schematic depiction of our proposed modulator is shown in Fig. 1, and we will explain it’s underlying properties in this chapter.

Fundamental structure of most integrated graphene based optical modulators is a planar capacitor [2, 8, 11], in which at least one electrode is graphene. In our proposed device graphene is used as both the top and the bottom electrode, but the following reasoning remains the same. The capacitor is used to electrically dope the graphene layer and shift its Fermi level thus controlling its absorption by tuning the graphene’s dynamic conductivity which is Fermi level dependent and given by the formula [12]:

\[
\sigma = \frac{\sigma_0}{2} \left( \tanh \left( \frac{\hbar \omega + 2E_F}{4k_BT} \right) + \tanh \left( \frac{\hbar \omega - 2E_F}{4k_BT} \right) \right),
\]

where \( \sigma_0 \) is the dynamic conductivity of intrinsic graphene equal to \( \sigma_0 = e^2/4\hbar = 60 \mu\text{S} \) [13]. In Eq. (1) we’ve included just the part of the dynamic conductivity corresponding to the inter-band transitions, as they are the only dominant ones at the standard \( \lambda = 1550 \text{ nm} \) communications wavelength on which we are focusing, when there is no initial, external, doping of graphene \( (E_F = 0 \text{ in initial state}) \). When the Fermi level is shifted to more than half of the input photon energy the dynamic conductivity of graphene falls to the 0 value as per Eq. (1), effectively annulling the graphene layer. Qualitatively, when electrical doping shifts the Fermi level to more than the half of the input photon energy, approximately all the available states bellow it are occupied and no further electrons can be absorbed in the case of \( n \) doping, or all the states above it are depleted in case of \( p \) doping, so no absorption can occur while preserving the momentum conservation law. This process is called the Pauli blocking and is schematically presented in Fig. 2(a) for the case of our proposed modulator.

The base structure of the modulator we are focusing on (a planar graphene capacitor with a thin dielectric) has been proposed previously [2, 8], but with
limited speed and energy consumption performance. In this work we prove that with our novelties in the design we can achieve a significant increase in the device speed and a reduction in energy consumption.

Since graphene modulators are based on a capacitor structure, it is clear that their speed and energy consumption are limited by the capacitor’s $RC$ constant, so in order to achieve greater speeds of the device, and lower power consumption, we need to reduce that constant as much as possible. The reduction of the device resistance requires advances in the fabrication process, but as we’ve emphasized in the introductory chapter that will not be the focus of this paper and the resistance value used in all calculations was taken from previously reported devices. On the other hand, the device capacitance can be greatly influenced by electromagnetic modeling and optimizations, and it is this reduction of the $C$ constant that is the main focus of this paper.

The plan capacitor formula is given as:

$$C = \varepsilon_0 \varepsilon_r \frac{wL}{d}. \quad (2)$$

In Eq. (2) $\varepsilon_r$ is the dielectric’s relative permittivity, $w$ is the width of the capacitor while $L$ is its length and $d$ the electrode distance. In order to reduce the capacitance, we need to focus on these structural parameters. We can observe that we can increase the capacitor’s thickness to achieve this goal, which, however, is not desirable due to the graphene’s $E_F(V)$ equation in parallel capacitor configurations [2], which is inversely proportional to $d$. If we increased the capacitor’s thickness we would require very high voltages to achieve switching which is not
optimal from the power consumption viewpoint. This is also the main reason of using the thin layer of aluminum oxide as the capacitor’s dielectric.

On the other hand, we can freely reduce the length and width of the capacitor and this is exactly what is achieved in the device we are proposing, shown in Fig. 1.

We propose the effective reduction of the width of the capacitor by utilizing the planar capacitor with the asymmetric, partial, overlap of the graphene electrodes. We are the first, to the best of our knowledge, to emphasize the importance of the overlapping electrode width, and we justify it through the following reasoning: When the electrodes are partially overlapped in a planar capacitor, the DC electric field will be confined just to the overlapping region as only there are the charges accumulated. Since the capacitance is proportional to the accumulated charge of the capacitor, the capacitor with overlapping electrodes can be equivalented by the capacitor of the width of the overlapping region (while the voltage remains the same) - the width of the capacitor is effectively reduced.

The effective reduction of the width of the capacitor has an undesirable side-effect - since the accumulation of charges is confined just to the overlapping region, and is proportional to the Fermi energy level, the Fermi energy shift is possible only in that region. This means that only the central part of graphene will have its absorption switched, while the parts near the edges of the waveguide will always be

![Fig. 2.](image-url) a) Magnified waveguide region with the modulator’s capacitor structure. The graphene’s band diagrams with charge distribution qualitatively depict the principle of operation of the modulator when the voltage is applied to the structure. b) Schematic depiction of the principle of operation of the modulator presented using the TM longitudinal electric field profiles.
absorptive and will constitute insertion loss. The impact of this drawback, however, is not significant in comparison to the benefit of the increased speed. As we’ve shown in our previous work [9], most of the absorption in the device occurs in the central region and not in the sides, due to the specific structure of the electric field which interacts with graphene. This principle of operation, as well as the mode profiles interacting with graphene are presented in Figs. 2(a) and 2(b).

The length of the device can be reduced by maximizing the controllable, graphene induced, absorption - when the absorption is maximized, smaller lengths are required to achieve the desired extinction ratios. In our previous work, we utilized a self-developed, graphene modified FDM method to characterize the absorption in graphene coated silicon waveguides, and have observed peaks in the TM mode absorption curves. In this paper, we extend this method to our newly proposed structure and use the absorption peaks to optimize the modulator design parameters. The absorption curves as well as the corresponding mode profiles of the modulator when no voltage is applied are shown in Fig. 3 (along with the absorption curve of just a single layer of graphene on a silicon waveguide [9]).

Result from Fig. 3 is used to optimize the dimensions of our device, as from it we can deduce that the optimal structural parameters of the device are $d = 240 \text{ nm}$ and $w = 600 \text{ nm}$. The absorption rate of the TM mode at the peak value is close to $0.3 \text{ dB/\mu m}$, which means that a structure of only $10 \text{ \mu m}$ length would be enough for a $3 \text{ dB}$ extinction ratio. It is this $3 \text{ dB}$ length that we use as the effective length of the modulator to significantly reduce its length, as well as to increase its speed and reduce the power consumption. The specified waveguide dimensions at which the

![Fig. 3.](image-url)

- a) Absorption dependency of waveguide thickness for different waveguide widths of the proposed graphene modulator (Dashed line: Absorption dependency of Single Layer Graphene on a silicon waveguide [9]).
- b) Optical mode profiles of the electric fields lying in the graphene plane for the TE and the TM modes, at the TM mode absorption peak dimensions.
TM mode absorption is maximized are emphasized in Fig. 1(b), and with the asymmetric capacitor constitute the main novelties of our proposal.

From the previous arguments, it can be deduced that the modulator we are proposing is polarization dependent, i.e. it is optimized for operation at the TM mode. Still, this kind of operation is typical for most integrated modulators [14] and additionally, with recent advances in integrated polarization rotators [15] we can assume that a very robust performance for all modes can be achieved.

Generally, we attribute the existence of the absorption peaks to the unique interaction between graphene and the TM longitudinal electric field (the only in-plane electric fields with which graphene interacts in the case of the TM mode, Fig. 2(b)), details of which we described in our previous work [9].

With these novel insights and proposals, we can significantly increase the modulator’s speed and reduce power consumption, as we confirm through numerical results presented in the following section.

## 3 Numerical results

In this chapter we present the numerical characterization of the newly proposed graphene based optical modulator on silicon. Since one of the main novelties in our proposal is the unique structure of the modulator, i.e. the asymmetric overlap of the graphene electrodes, all the numerical results are presented as function of the overlapping width $w_G$, as shown in Figs. 4 and 5.

Fig. 4(a) exhibits the total, calculated, graphene induced absorption, the insertion loss arising from the non-modulating far ends of the graphene electrodes and the resulting total modulation depth. As a remainder, we are focusing on the TM mode and have chosen the dimensions of the silicon waveguide to correspond to the TM mode absorption peaks observable in Fig. 3. These dimensions are $d = 240$ nm for the thickness of the waveguide and $w = 600$ nm for the width. We can observe that the modulation depth calculated when the electrodes are covering the entire area of the waveguide (i.e. $w_G = w = 600$ nm) is 0.28 dB/$\mu$m, and this is the highest reported modulation depth of any graphene based device up to date, to the best of our knowledge.

In Fig. 4(a) we can also observe that the reduction in the overlapping width does not have a significant impact on the insertion loss even for relatively small overlapping region values. It is not until the overlapping width decreases to around the third of the width of the waveguide that the insertion loss becomes significant.

Fig. 4(b) shows the calculated length of the device required to achieve 3 dB modulation depth based on the modulation depth per micrometer introduced in Fig. 4(a), and the corresponding total insertion loss resulting from the non-modulating graphene. As we emphasized in the previous chapter, we are assuming that the 3 dB length is enough for a fully-functioning device, and take is as the length of the modulator. We acknowledge that this approximation might not be fully appropriate, but still argue that in combination with other integrated photonic elements the total modulation depth could be significantly amplified, and that the high speed and low energy consumption remain the main goals for a graphene based modulator. Regarding the total insertion loss, we can observe that more than
half of the waveguide can withstand the non-modulating graphene, while the total insertion loss remains below 1 dB. This is all due to the special form the longitudinal electric field interacting with the graphene layer in the case of the TM mode.

After calculating the 3 dB length and taking it as the length of the device, we are able to calculate the main property of the modulator that we are trying to minimize, its capacitance $C$. We obtain it using Eq. (3) and taking the width of the overlapping region as the width of the waveguide, as per the discussion introduced in the previous chapter. Capacitance of the modulator with respect to the width of the overlapping region is shown in Fig. 5(a). We can observe that the reduction in capacitance arising from the decrease in the overlapping region width is not negligible.

Using the calculated capacitance, we can estimate the dynamic response of the modulator using the equation [16]:

$$ B = \frac{1}{2\pi RC}. $$

(3)

As mentioned in previous chapters, we assume no advances in the fabrication processes so the resistance of the modulator we have used in our simulations equals the resistance of the previously reported graphene based modulator on a silicon waveguide of $R = 250 \Omega$ [11], which exhibited the highest speed.

![Fig. 4. a) Graphene induced absorption and insertion loss dependency of the overlapping width $w_G$, with emphasized modulation depth. b) The 3 dB length and corresponding total insertion loss dependency of the overlapping width $w_G$.](image)
The dynamic response of the modulator is shown in Fig. 5(b). The highest reported speed of a graphene modulator on a silicon waveguide to date, using this kind of structure, has been the $B = 10 \text{Gb/s}$ [11], but as we can observe in Fig. 5(b), just from introducing the optimizations to the waveguide dimensions to maximize the absorption for the TM mode, and by paying attention that the graphene electrodes overlap just above the waveguide region (i.e. $w = w_G$), we can obtain the speed of $B = 20 \text{Gb/s}$, which is already twice as high. By making further design updates through the reduction of the overlapping width of the graphene electrodes, we can extend the peak of the speed of the modulator to up to $B = 30 \text{Gb/s}$.

While there have recently been proposals of graphene based modulator reaching similar speeds [7], all of them employ fabricating more complex structures to utilize specific properties of graphene, while our proposal is based on pure EM optimizations and is easier to fabricate and integrate with other components. Furthermore, with only slight advances in the fabrication process (reduction of the $R$ constant), the speed of our modulator could reach 100 Gb/s, enough for all on-chip optical communications.

The other very important parameter which directly depends on the capacitance of the device is the energy consumption, described by the energy-per-bit equation given by the formula [17]:

$$E_b = \frac{1}{4} C_{tot} V_R^2$$

$$B \approx \frac{1}{2\pi R C_{tot}}$$
where $C$ is the capacitance of the modulator, while $V_{PP}$ is the peak-to-peak voltage required to switch the modulator. It is clear from Eq. (4) that the reduction of the capacitance leads directly to the decrease in the energy consumption, while at the same time increasing the speed of the device. Energy per bit calculated for our device is presented in Fig. 5(b).

The only unknown parameter in Eq. (4) is the peak-to-peak voltage required to achieve full modulation. We calculated this voltage as $V_{PP} = 4.12 \, \text{V}$ using the Fermi level dependency of the applied voltage equation in graphene capacitors [2], where we assumed the required Fermi energy to be achieved is 0.4 eV as it is exactly half of the photon energy at our target wavelength of $\lambda = 1550 \, \text{nm}$. This is the energy required to achieve complete Pauli-blocking. Peak to peak voltage of $V_{PP} = 4.12 \, \text{V}$ was calculated, assuming a zero bias voltage, which is the worst-case scenario threshold and a good starting point to estimate power consumption.

As we can observe from Fig. 5(b), the energy-per-bit of our proposed device has values between $E_b = 140 \, \text{fJ/bit}$ to as low as $E_b = 90 \, \text{fJ/bit}$, depending on the width of the overlapping region. These values are record low in comparison with other devices, all-silicon photonic or hybrid [8, 18]. One of the crucial conditions for large scale integration of silicon photonic components, is to have the power consumption below $E_b = 100 \, \text{fJ/bit}$, as only then could silicon photonic interconnections truly be more sufficient than the copper ones, in power consumption, as well as in speed. This has traditionally been the problem of all-silicon photonic devices, and also silicon photonic - graphene hybrid devices, but as we show in this paper, using electromagnetic optimizations on the design of the graphene modulator we can achieve all the required criteria for an ultra-efficient device with a potential application in optical interconnects and large scale photonic integrated circuits.

Another big benefit of the optimizations of the graphene modulator design to increase speed and reduce power consumption, which wasn’t emphasized in the previous sections but was implied and is highly important, is that the footprint of the device is also reduced significantly, which is crucial for use in short range optical interconnects. The footprint of our proposed device would be equal to the chosen 3 dB length multiplied by the distance between the electrodes, which is just slightly larger than the width of the waveguide (the electrodes need to be far enough from the waveguide as not to disturb the optical mode, but this distance is proven to be very small [3]). Thus if we assume the lateral size of the modulator is $1 \, \mu\text{m}$, the footprint can be as small as $10 \, \mu\text{m}^2$, which is much smaller than the footprint all previously proposed graphene modulators [2, 7, 8], and by extension much smaller than the all-silicon modulators fabricated in the MZM configuration [18]. This large reduction in the footprint and energy consumption of graphene modulators, along with the increase in speed, could be the propelling property which would definitely make graphene modulators a competitor to the standard integrated modulators of today.
4 Conclusion

In this paper, we proposed a novel structure for the two-layer graphene optical modulator on silicon, and proved through numerical simulations that with optimizations in the graphene capacitor design, we can reach speed and energy performances which surpass the ones of established graphene-based modulators, and are comparable to, or surpass, the all-silicon devices. Furthermore, we proved that all of this is achievable just based on a deeper understanding of the underlying physical processes of the graphene’s light matter interaction, and doesn’t require additional advances in the fabrication methods.

We hope these results will spark further interested in graphene based integrated optics, and will influence the creation of robust, integrated, commercially applicable optical systems based on graphene.

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