High-performance compound-semiconductor integrated circuits for advanced digital coherent optical communications systems

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Abstract: Communications traffic over photonic networks is exponentially increasing due to the spread of broadband applications. To cope with the rapid growth, novel 100-Gb/s digital coherent systems have been deployed recently in optical core networks. Further research and development of digital coherent technologies with channel rates of beyond 100 Gb/s is now being conducted. Optical transceivers for such high-speed communications systems need high-performance analog and mixed-signal electronic circuits such as optical modulator drivers, transimpedance amplifiers (TIAs), analog-to-digital converters (ADCs), and digital-to-analog converters (DACs). Compound-semiconductor integrated circuits (ICs) have played key roles in this technical field. This paper reviews recent trends in compound-semiconductor ICs for such advanced digital coherent optical communications systems and presents our latest results based on InP heterojunction bipolar transistor (HBT) technology.

Keywords: compound-semiconductor IC, optical communication, digital coherent, ADC, DAC, modulator driver, TIA, InP HBT

Classification: Electron devices, circuits and modules

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1 Introduction

The amount of data traffic in optical communications networks continues to grow exponentially due to the spread of broadband applications and services such as video streaming and cloud computing. The architecture of optical networks in Japan is shown in Fig. 1. In the core networks in particular, huge-capacity and long-haul transmission technologies are required in order to accommodate client data and to link metropolitan areas. Trends in the transmission capacity per optical fiber of the core networks are shown in Fig. 2. In the early stage, electrical time-division multiplexing (TDM) based on on-off keying (OOK) was the main technique used to increase transmission capacity. In the 1990s, wavelength-division multiplexing (WDM) was introduced, leading to rapid progress in increasing the transmission capacity. Then, 40-Gb/s × 40-wavelength (or -channel) systems were deployed, and the total transmission capacity reached 1.6 Tb/s.

To cope with the increasingly rapid growth of communications traffic, innovative 100-Gb/s digital coherent technology [1, 2], which combines coherent detection and digital signal processing (DSP), has recently been introduced. Digital

Fig. 1. Architecture of optical networks in Japan.

Fig. 2. Trends in transmission capacity of core networks.

coherent technology enables us to employ a variety of spectrally efficient modulation formats such as phase shift keying (PSK) and quadrature amplitude modulation (QAM). Moreover, we can utilize equalization techniques for compensating transmission impairments in the digital domain.

In the latest practical digital coherent systems, 100-Gb/s channel capacity is achieved by using polarization division multiplexed (PDM) quadrature phase shift keying (QPSK) at a symbol rate of 32 Gbaud, which includes forward error correction (FEC) redundancy [3]. To further increase the channel capacity, the technology needs to expand along three axes as shown in Fig. 3: the number of multilevels, the number of subcarriers, and the symbol rate. The next-generation 400-Gb/s system will be developed by using two-subcarrier 32-Gbaud PDM 16-ary QAM (16QAM) and will be put into practical use in the near future [4]. Attention is already moving to 1-Tb/s/channel-class technologies [5]. A higher symbol rate is now attracting attention for 1-Tb/s systems.

Fig. 3. Three axes for increasing channel capacity.

The transceivers for such advanced high-speed digital coherent systems are composed of not only optical components but also high-performance electronic circuits such as a large-scale DSP, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), optical modulator drivers, and transimpedance amplifiers (TIAs). Compound-semiconductor III–V technologies such as InP heterojunction bipolar transistors (HBTs) have provided key functions in the coherent transceiver, especially in the high-speed analog and mixed-signal building blocks.

This paper reviews recent progress in compound-semiconductor integrated circuits (ICs), mainly III–V ICs, for advanced digital coherent optical communications. In Section 2, we present an overview of materials and technologies for high-performance ICs. In Section 3, we describe recent trends in circuit technologies for digital coherent transceivers. In Section 4, we introduce our recent results based on InP HBT technology for coherent applications. Section 5 concludes our review.

2 Materials and technologies for high-performance ICs

Fig. 4 plots the properties of several major semiconductor materials and technologies for the high-speed ICs. They are roughly mapped in the graph showing Johnson's figure-of-merit (FOM) (product of transistor cutoff frequency and breakdown voltage [6]) versus scale of integration (transistor count) [7]. Compound-semiconductor technologies such as GaAs-, InP-, and GaN-based transistors have superior Johnson's FOM compared to Si-based technologies because of their inherent high electron mobility or wide energy bandgap [8]. Therefore, compound semiconductors have driven performance advancements in analog and mixed-signal ICs for various applications such as optical and wireless communications systems. For example, the cutoff frequency (f_t) and maximum oscillation frequency ($f_{\max}$) of InP-based transistors have reached above 700 GHz [9] and 1 THz [10], respectively.

In contrast, Si CMOS is obviously superior technology in terms of the scale of integration, functionality, and levels of yield and manufacturability. Additionally, continuous scaling has driven device speeds of RF CMOS [11] and SiGe HBTs into the multi-100-GHz region at the expense of breakdown voltage. Although the f_t and $f_{\max}$ of transistors in recent nanoscale CMOS and SiGe technologies are nearly comparable to those of InP-based transistors, the metal backend is usually not as good for making passive components such as transmission lines. In particular, the InP-based technologies have a much higher resistivity substrate, and thus, they are more suitable for making low-loss passive components, which minimizes parasitic capacitance and noise coupling through the substrate.

Fig. 4. Technology mapping: Johnson's FOM versus scale of integration.

As above, each material and technology has its superior properties. We need to choose the appropriate ones for implementing in circuits by considering the requirements for the target applications, for example, functionality, bandwidth, signal amplitude or dynamic range, power consumption, and cost effectiveness. In the following section, the case of advanced digital coherent optical communications is addressed.

3 High-performance circuits for digital coherent transceiver

Block diagrams of a transmitter and a receiver for digital coherent systems are shown in Fig. 5. The transmitter consists of a DSP, DACs, optical modulator drivers, optical I/Q modulators, a laser diode (LD), and optical circuits. In contrast, the receiver is composed of a DSP, ADCs, TIAs, photodiodes (PDs), a local

Fig. 5. Block diagrams of digital coherent transceiver: (a) transmitter, and (b) receiver.

oscillator (local LD), and optical circuits. Not only the optical components but also high-speed electronic circuits play key roles in the digital coherent transceiver. In the following subsections, we briefly summarize the recent trends for the DSP, data converters (DAC and ADC), modulator driver, and TIA.

3.1 DSP

The DSP for digital coherent systems must have many functions such as FEC encoding and decoding, fixed equalization for chromatic dispersion compensation, and adaptive equalization for polarization demultiplexing and polarization mode dispersion compensation. The functions of the DSP for digital coherent systems are described in detail in [3, 12].

The nanoscale CMOS technology is an obvious choice for the DSP to ensure such high functionality while maintaining low power consumption. For example, the pioneer DSPs for 100-Gb/s digital coherent systems were fabricated using 40-nm and 20-nm CMOS technology [3, 12]. In addition, DSPs for beyond-100 Gb/s systems fabricated with 16-nm CMOS (FinFET) technologies have been announced very recently [13, 14].

3.2 Data converters: DAC and ADC

Digital coherent transceivers require very high-performance DACs and ADCs in order to generate and detect complex modulated signals at a high symbol rate. For example, a resolution of more than 6 bits and a sampling rate of over 64 GS/s, assuming two samples/symbol operation, are required for current 100-Gb/s (32-Gbaud PDM QPSK) and next-generation 400-Gb/s (2-subcarrier 32-Gbaud PDM 16QAM) systems. In addition to such a high sampling rate, analog bandwidth of around 20 GHz, which is greater than the Nyquist frequency of the symbol rate of 32 Gbaud, is also required. Moreover, a higher sampling rate and broader bandwidth will be required for 1-Tb/s-class systems with a higher symbol rate.

State-of-the-art high-speed data converters are summarized in Tables I and II (DACs in Table I, ADCs in Table II) and in Fig. 6. High-performance DACs and ADCs have already been demonstrated in nanoscale CMOS technologies [15, 17, 19, 21, 22, 23] and been put into practical use. They have high sampling rates but limited analog bandwidth of less than about 20 GHz. To overcome this analog bandwidth limitation of CMOS-based technology, InP- or SiGe-HBT-based converters have also been investigated [16, 18, 20, 24] for 1-Tb/s-class systems. In addition, InP- or SiGe-based ultra-broadband track-and-hold amplifiers (THAs) [25, 26] and analog multiplexers (AMUXs) [27] have attracted attention for their ability to enhance the analog bandwidth of CMOS-based data converters as a more practical approach for digital coherent transceivers. In section 4, we describe the details of our over-40-GHz-bandwidth 90-GS/s DAC [20] and over-50-GHz-bandwidth AMUX [27] in InP HBT technology.

Table I. High-speed DACs

Ref.	[15]	[16]	[17]	[18]	[19]	[20]	[21]
Publication	2011	2011	2012	2014	2014	2015	2016
Material	Si	InP	Si	SiGe	Si	InP	Si
Technology	CMOS	HBT	CMOS	BiCMOS	CMOS	HBT	CMOS
Node	65-nm	0.5- μ m	40-nm	-	28-nm	0.5- μ m	-
ft/fmax (GHz)	-/-	290/320	-/-	-/-	-/-	290/320	-/-
Topology	SEG (TRM+BW)	R-2R	SEG	-	SEG (TRM+BW)	R-2R	-
Resolution	6	6	8	6	8	6	8
Sampling rate (GS/s)	56	60	65	72	100	90	85
Analog bandwidth (GHz)	-	>30	13	23	13	>40	>15
Power dissipation (W/ch.)	0.75	1.8	0.75	19.5 (DAC core: 0.6 W)	2.5	3.4 (DAC core: 0.5 W)	-
Max. output amplitude (mVppd)	540	1000	700	1800	900	1000	-
Target application	100 G	400 G	100 G	400 G	100 G/400 G	1 T	400 G

SEG: segmented architecture, TRM: thermometer-coded architecture, BW: binary-weighted architecture,
R-2R: R-2R ladder architecture

Table II. High-speed ADCs

Ref.	[22]	[23]	[24]	[21]
Publication	2012	2014	2015	2015
Material	Si	Si	SiGe	Si
Technology	CMOS	CMOS (SOI)	BiCMOS	CMOS
Node	40-nm	32-nm	-	-
ft/fmax (GHz)	-/-	-/-	-/-	-/-
Topology	SAR/TI	SAR/TI	TI	-
Resolution	8	8	6	8
Sampling rate (GS/s)	65	90	68	85
Analog bandwidth (GHz)	20	22	>25	>20
Power dissipation (W/ch.)	1.2	0.67	-	-
Input amplitude (mVppd)	700	700	400	-
Target application	100 G	100 G/400 G	400 G	400 G

SAR: successive approximation architecture,
TI: time interleaved architecture

Fig. 6. High-speed DACs and ADCs for digital coherent systems.

3.3 Optical modulator driver

LiNbO₃-based Mach-Zehnder modulators (MZMs) are widely used in the optical I/Q modulator for current 100-Gb/s digital coherent systems because of their low loss and broadband characteristics [28]. They need a driving voltage above 6 V. Therefore, the modulator driver must have broad bandwidth, high gain, and large output amplitude of more than 6 V. To lower the power consumption and make the transceiver compact, InP-based MZMs are being developed for next-generation systems [29]. InP-based MZMs have a smaller size and lower driving voltage than LiNbO₃-based ones, but they still need a driving voltage above 3 V. In addition, the linearity has become a more important specification for next-generation systems with higher-order multilevel modulations such as 16QAM.

III–V technologies such as GaAs pHEMTs and InP HBTs are applicable choices for implementing the broadband and large-output-amplitude modulator drivers. In fact, almost all the commercial modulator drivers for digital coherent application have so far been based on GaAs pHEMTs or InP HBTs. Table III

lists the recently reported optical modulator drivers for digital coherent application [30, 31, 32, 33, 34]. InP-HBT-based drivers have attracted attention because of their broad bandwidth characteristics for beyond-100-Gb/s systems. We have demonstrated a 36-GHz-bandwidth driver module in 0.5- μm InP HBTs [33] and an over-67-GHz driver IC in 0.25- μm InP HBTs [34] for 400-Gb/s and 1-Tb/s-class systems.

Table III. Parameters of optical modulator drivers

Ref.	[30]	[31]	[32]	[33]	[34]
Publication	2012	2012	2014	2015	2016
Material	GaAs	InP	InP	InP	InP
Technology	pHEMT	HBT	HBT	HBT	HBT
Node	0.15- μm	2- μm	-	0.5- μm	0.25- μm
f _t /f _{max} (GHz)	100/-	100/175	150/200	290/320	400/450
Breakdown voltage (V)	14	19	-	>4	>3.5
Driver Type (Input-Output)	Limiting (Single-Single)	Limiting (Single-Single)	Linear (Diff.-Diff.)	Linear (Diff.-Diff.)	Linear (Diff.-Diff.)
Max. gain (dB)	30	>32	12.5	15	10.7
Bandwidth (GHz)	32 (packaged)	-	45 (on wafer)	36 (packaged)	>67 (on wafer)
Max. output amplitude (V _{pps} or V _{ppd})	8	9	>2.5	>3	>2
THD (%)	-	-	3	3	-
Power dissipation (W/ch.)	2.4	3.5	0.60	0.83	0.84
Functions	- Amp. control - Cross-point control	- Amp. adjust	-	-Amp. control (Gain control)	-Amp. control (Gain control)
Target application	100 G (LN MZM)	100 G (LN MZM)	100 G/400 G (InP MZM)	100 G/400 G (InP MZM)	400 G/1 T (InP MZM)

THD: total harmonic distortion, LN MZM: LiNbO₃-based Mach-Zehnder modulator, InP MZM: InP-based Mach-Zehnder modulator

3.4 TIA

On the receiver side, TIAs are key components for converting a varying current signal from PDs into a constant voltage signal. TIAs for the digital coherent application are required to have a high gain-bandwidth product, low noise characteristics, and good linearity to ensure a wide dynamic range and high sensitivity. Additionally, many externally controllable functions such as output amplitude adjustment, output shutdown, and automatic/manual gain control (AGC/MGC) switching are also needed [35].

TIAs recently reported for digital coherent systems are listed in Table IV [36, 37, 38, 39, 40]. To achieve both high gain-bandwidth product and high functionality, an InP HBT or SiGe HBT is selected for TIA circuit implementation. A 68-GHz-bandwidth TIA using InP HBT technology has been demonstrated for 1-Tb/s-class systems [39].

Table IV. TIAs used in digital coherent systems

Ref.	[36]	[37]	[38]	[39]	[40]
Publication	2011	2012	2014	2015	2016
Material	InP	InP	SiGe	InP	SiGe
Technology	HBT	HBT	BiCMOS	HBT	BiCMOS
Node	1- μ m	1- μ m	0.13- μ m	0.7- μ m	0.13- μ m
$f_t/f_{\max}$ (GHz)	170/270	170/270	200/265	400/370	250/300
Z _t (dB Ω)	68	77	80	59	80
Bandwidth (GHz)	23	25.1	24	68.1	53
THD (%)	-	<3.3	1.2	-	<5
I _{eq} (pA/ $\sqrt{\text{Hz}}$)	-	-	24	22	24.86
Power dissipation (mW/ch.)	660	430	350	475	277
Max. output amplitude (mV _{ppd})	540	>800	700	700	900
Functions	- AGC - Peak detector - AOC	- AGC/MGC - Peak detector - AOC - Amp. control - Output shutdown	- SPI interface - AGC/MGC - Peak detector - Amp. control - Output shutdown - BW control - Peaking control	- MGC - BW control	- AGC/MGC - Peak detector - Amp. control
Target application	100 G	100 G	100 G	400 G/1 T	100 G/400 G

Z_t: trans-impedance gain, THD: total harmonic distortion, I_{eq}: input-referred current noise, AGC: automatic gain control, MGC: manual gain control, AOC: automatic offset cancellation

4 High-performance InP-HBT ICs

As mentioned in the previous section, InP-HBT ICs have provided key functions in digital coherent transceivers, especially in the analog and mixed-signal building blocks. In this section, we introduce our recent results using in-house InP HBT technology.

4.1 InP HBT technology

We have developed InP HBT technology for fabricating high-speed analog and mixed-signal ICs. Our reliable 0.5- μ m-emitter-width InP HBTs have peak f_t and $f_{\max}$ values of 290 and 320 GHz, respectively (Fig. 7(a)). The HBTs utilize a thin InP emitter layer suitable for making thin passivation ledge structures, thus enhancing device reliability [41]. A thin n-type doped layer is also utilized in the heterojunction vicinity to lower the turn-on voltage, $V_{\text{BE,ON}}$, of the transistor. The turn-on voltage is approximately 0.75 V for $J_C = 1 \text{ mA}/\mu\text{m}^2$. The fabricated HBTs exhibit a current gain of over 100. The breakdown voltage, BV_{CEO} , is approximately 4 V. The technology also features three metal interconnect layers, metal-insulator-metal (MIM) capacitors, thin-film resistors, and backside ground vias. Low-permittivity benzocyclobutene (BCB) was used as the isolating layer between the interconnections.

In addition, we recently developed 0.25- μ m-emitter-width InP HBT technology [42]. The fabricated 0.25- μ m HBTs exhibit current gain of over 30 and $f_t/f_{\max}$ of over 400/450 GHz at J_C of $10 \text{ mA}/\mu\text{m}^2$, as shown in Fig. 7(b).

Fig. 7. RF performance: (a) 0.5- μm InP HBT, and (b) 0.25- μm InP HBT.

4.2 Optical modulator drivers using 0.5- and 0.25- μm InP HBTs

We designed and fabricated a broadband linear optical modulator driver with 0.5- μm InP HBT technology [33]. A block diagram of the driver is shown in Fig. 8. The driver has a fully differential two-stage configuration comprising a lumped variable-gain amplifier (VGA) and distributed output buffer. The VGA is based on the Gilbert-cell structure and has a gain control range of over 15 dB. For the output buffer, we used a distributed configuration to achieve both a large output swing of 3 V_{ppd} and good output return loss. The output buffer is composed of six unit cells. Each cell is based on emitter-followers and a differential pair as shown in Fig. 9.

Fig. 8. Block diagram of driver.

Fig. 9. Schematic of cell.

Fig. 10 shows photographs of a driver IC and a module based on a surface mount (SMT) package. In the digital coherent transmitter, four-channel driver functions are required in total for PDM I/Q modulation. To reduce the size of the driver module, the IC has two channels on one chip. The module has two two-channel ICs and thus has four-channel functions.

The measured small-signal characteristics of the driver module are plotted in Fig. 11. At the maximum gain condition, the f-3 dB bandwidth and differential gain are 36 GHz and 15 dB, respectively. At the minimum gain condition, they are 36 GHz and -4 dB. The inter-channel crosstalk is better than -20 dB in the f-3 dB

Fig. 10. Photographs of (a) dual-channel driver IC, and (b) quad-channel driver module.

Fig. 11. Measured small-signal characteristics: (a) S-parameters, and (b) inter-channel crosstalk.

Fig. 12. Measured large-signal output waveforms: (a) NRZ @32 Gbaud, (b) PAM4 @ 32 Gbaud, and (c) NRZ @ 50 Gbaud.

bandwidth range. Fig. 12 shows the measured large signal output waveforms. We obtained clear non-return to zero (NRZ) and 4-level pulse amplitude modulation (PAM4) waveforms at 32 Gbaud and 50 Gbaud. The power consumption was as low as 0.83 W/ch.

Thus, this driver module is applicable for 100-Gb/s and 400-Gb/s-class digital coherent systems. To the best of our knowledge, this quad-channel driver module has the broadest bandwidth and the smallest size of any previously reported SMT-packaged drivers.

In addition, we recently succeeded in enhancing the bandwidth of the driver IC using newly developed 0.25- μm InP HBTs [34]. The circuit configuration is the same as that of the driver with 0.5- μm InP HBTs. Fig. 13 shows a photograph of

the driver IC using 0.25- μm InP HBTs. The driver has an f-3 dB bandwidth of over 67 GHz, which is the upper limit of our measurement setup, and a differential gain of 10.7 dB as shown in Fig. 14(a). We obtained clear output waveforms of NRZ at 100 Gbaud and PAM4 at 56 Gbaud (Fig. 14(b), (c)). This driver IC is promising for 1-Tb/s-class systems with higher symbol rates.

Fig. 13. Photograph of driver IC.

Fig. 14. Measured characteristics of (a) S-parameters, (b) NRZ @ 100 Gbaud, and (c) PAM4 @ 56 Gbaud.

4.3 40-GHz-BW 90-GS/s 6-bit DAC using 0.5- μm InP HBTs

We have developed an ultra-broadband DAC in 0.5- μm InP HBT technology [20]. A block diagram of the DAC IC is shown in Fig. 15(a). The IC includes twelve D-FFs, six 2:1 MUXs, and a DAC core. The D-FFs are inserted at the first stage to retiming and reshape the digital input signals. The 2:1 MUXs multiplex the twelve half-rate digital signals into six full-rate digital signals. Then the DAC converts the six digital signals into an analog signal. With this structure, the DAC operates with a half-rate clock. This leads to relaxed speed restraints for clock distribution and a higher sampling-rate operation compared with a conventional full-rate-clock structure. The DAC core is based on an R-2R ladder current-steering architecture as shown in Fig. 15(b). The R-2R ladder-based architecture is an appropriate choice to achieve high-speed and low-power operation for medium-resolution InP-HBT DACs [16]. The value of the resistor, R , in the ladders is set to 50 ohm to make the output impedance of the DAC 50 ohm. The ladder is implemented with a combination of unit resistors for good relative matching. The current-switch cell is based on a differential pair with emitter-degeneration resistor. To achieve broadband characteristics, the switching transistors in the cell are biased at peak f_t current

density and proper collector-base voltage to lower the collector capacitance. In addition, we used transistor current sources with large emitter degeneration in the cell to achieve good relative current matching and achieve high impedance.

Fig. 15. (a) Block diagram of DAC IC, and (b) schematic of DAC core.

A photograph of the DAC IC is shown in Fig. 16(a). The chip size is 3 mm × 3 mm. The IC consumes a total power of 3.4 W with a supply voltage of −4.0 V. More than 80% of the power is consumed by the retiming and multiplexing function blocks. The DAC core consumes only 0.5 W. Fig. 16(b) shows a photograph of the DAC test module. To ensure the broadband characteristics, we employed 1-mm connectors, which cover the frequency range from DC to 110 GHz, for the analog output ports. The SMPM connectors, which cover the range up to 65 GHz, are applied to digital and clock input ports.

Fig. 16. Photographs of (a) DAC IC, and (b) DAC test module.

The DAC module has a full-scale output amplitude of 1 V_{ppd}. Fig. 17 plots the measured output amplitude versus output frequency. Each plot was measured under

the full Nyquist operating condition with a full-scale 0–1 output pattern. The module has an excellent broad bandwidth of over 40 GHz and operates at sampling rates of up to 90 GS/s. Fig. 18(a) and (b) show the measured PAM4 signals at symbol rates of 50 Gbaud and 75 Gbaud, respectively. Thanks to the ultra-broad-band characteristics of the module, we obtained clear PAM4 signals at symbol rates up to 75 Gbaud without any pre-emphasis techniques. Additionally, we have succeeded in demonstrating WDM transmission of 1-Tb/s (two-subcarrier 75-Gbaud PDM 16QAM) signals over 1,920 km [43] using this ultra-broadband DAC module. Thus, this DAC module can be applied to 1-Tb/s-class digital coherent transmission.

Fig. 17. Measured output amplitude versus output frequency.

Fig. 18. Measured PAM4 waveforms: (a) 50 Gbaud, and (b) 75 Gbaud.

4.4 50-GHz-BW AMUX using 0.5- μ m InP HBTs

InP-HBT-based DACs [16, 20] obviously have a broader analog bandwidth than CMOS-based DACs, and they are suitable for signal generation at a high symbol rate. However, there seems to be some difficulty in connecting or integrating them with the DSPs due to the complexity of their interface. Therefore, a strong demand exists for increasing or extending the analog bandwidth of CMOS-based DACs. We recently devised a new method to double the analog bandwidth of CMOS-based DACs using an InP-HBT-based analog multiplexer (AMUX) [27]. Fig. 19 shows a block diagram of the AMUX IC. It consists of two input linear buffers, a clock buffer, an AMUX core, and an output linear buffer with 50-ohm termination resistors. All the building blocks have fully differential architectures. The AMUX core is based on a simple selector circuitry. To ensure the linear operation, we

inserted emitter-degeneration resistors in the upper differential pairs for analog signals, as shown in Fig. 20. The transistors in the core circuit are biased at peak f_t current density and proper collector-base voltage to achieve the broadband and fast switching operation. We used a cascode circuit topology for the output buffer to reduce the Miller effect and to improve the bandwidth.

Fig. 19. Block diagram of AMUX IC.

Fig. 20. Schematic of AMUX core.

Fig. 21(a) shows a microphotograph of the A-MUX IC. The chip size is 2×2 mm. The IC's total power consumption is 0.5 W at a single power supply voltage of -4.5 V. Fig. 21(b) shows a photograph of the A-MUX test module. This AMUX module has through bandwidth of over 50 GHz as shown in Fig. 22.

Fig. 21. Photographs of (a) AMUX IC, and (b) AMUX test module.

Fig. 22. Measured S-parameters of AMUX module in through-mode.

We devised a novel concept to double the bandwidth of CMOS-based DACs using the AMUX. The principle of this technique, which we call a digital-preprocessed analog-multiplexed DAC (DP-AM-DAC), is shown in Fig. 23. The DP-AM-DAC consists of a digital preprocessor, two sub-DACs with a limited bandwidth of $f_c/2$, and an AMUX with a bandwidth greater than f_c . In the digital preprocessing, the target signal is separated into upper- and lower-band signals around the frequency of $f_c/2$. The upper-band signal is emphasized by a factor of $1/r$, where the value of “ r ” depends on the shape of the clock signal for the AMUX. The complex conjugate of the emphasized upper-band signal is flipped around $f_c/2$ and added to the lower-band signal with the phases of 0 and 180 degrees. These two signals for sub-DACs have a signal bandwidth of around $f_c/2$ so that the sub-DACs can convert them into analog signals without an information penalty. Finally, the outputs from the sub-DACs are multiplexed at a clock rate of f_c by the AMUX. Thus, we can obtain the arbitrary signals with a bandwidth of f_c , which is twice that of the bandwidth of sub-DACs. In this scheme, a residual image appears in the upper frequency range ($>f_c$), but it can be easily removed by filtering. More details of the DP-AM-DAC are described in [44].

Fig. 23. Principle of bandwidth-doubling technique based on DP-AM-DAC.

For the proof of concept, we demonstrated a signal generation of 80 Gbaud (160-Gb/s) Nyquist PAM4 based on 20-GHz-bandwidth sub-DACs (arbitrary

waveform generators) and the AMUX module. In this measurement, the AMUX operated at a clock rate of 43.3 GHz. As shown in Fig. 24, we succeeded in doubling the analog bandwidth of DACs and generating 80-Gbaud PAM4 signals. Additionally, we recently demonstrated WDM transmission of 96-Gbaud PDM-QPSK signals over 12,120 km [45] based on this bandwidth-doubling technique using InP-HBT AMUX.

Thus, the AMUX-based bandwidth-doubling technique is promising for future high-symbol-rate optical communications systems.

Fig. 24. Demonstration of 80-Gbaud PAM4 signal generation.

5 Conclusion

Recent trends and progress in compound-semiconductor ICs and our latest results based on InP HBT technology for advanced digital coherent optical communications systems were reviewed. Compound-semiconductor ICs have played important roles in digital coherent transceivers, especially in the optical modulator drivers and TIAs, which are required to have ultra-broadband, high-gain, large-output amplitude, and low-noise/distortion characteristics. Ultra-broadband AMUXs and THAs would be key components for enhancing the analog bandwidth of CMOS-based data converters for 1-Tb/s-class systems with higher symbol rates. Compound-semiconductor ICs will continue to serve key functions for high-end optical communications systems.

Compound-semiconductor technologies have much potential for enhanced performance and will continue to drive advancements in analog and mixed-signal ICs for various applications and systems.

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